

# MF CV520

## Contactless reader IC

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219710

Objective data sheet  
COMPANY PUBLIC

## 1. Introduction

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This document describes the functionality and electrical specifications of the contactless reader/writer MF CV520.

**Remark:** The MF CV520 supports all variants of the MIFARE Mini, MIFARE 1K, MIFARE 4K, MIFARE Ultralight, MIFARE DESFire EV1 and MIFARE Plus RF identification protocols. To aid readability throughout this data sheet, the MIFARE Mini, MIFARE 1K, MIFARE 4K, MIFARE Ultralight, MIFARE DESFire EV1 and MIFARE Plus products and protocols have the generic name MIFARE.

## 2. General description

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The MF CV520 is a highly integrated reader/writer IC for contactless communication at 13.56 MHz. The MF CV520 reader supports ISO/IEC 14443 A/MIFARE mode.

The MF CV520's internal transmitter is able to drive a reader/writer antenna designed to communicate with ISO/IEC 14443 A/MIFARE cards and transponders without additional active circuitry. The receiver module provides a robust and efficient implementation for demodulating and decoding signals from ISO/IEC 14443 A/MIFARE compatible cards and transponders. The digital module manages the complete ISO/IEC 14443 A framing and error detection (parity and CRC) functionality.

The MF CV520 supports MF1xxS20, MF1xxS70 and MF1xxS50 products. The MF CV520 supports contactless communication and uses MIFARE higher transfer speeds up to 848 kBd in both directions.

The following host interfaces are provided:

- Serial Peripheral Interface (SPI)

## 3. Features and benefits

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- Highly integrated analog circuitry to demodulate and decode responses
- Buffered output drivers for connecting an antenna with the minimum number of external components
- Supports ISO/IEC 14443 A/MIFARE
- Typical operating distance in Read/Write mode up to 100 mm depending on the antenna size and tuning
- Supports MF1xxS20, MF1xxS70 and MF1xxS50 encryption in Read/Write mode
- Supports ISO/IEC 14443 A higher transfer speed communication up to 848 kBd
- Supports MFIN/MFOU

- Supported host interfaces
  - ◆ SPI up to 10 Mbit/s
- FIFO buffer handles 64 byte send and receive
- Flexible interrupt modes
- Hard reset with low power function
- Power-down by software mode
- Programmable timer
- Internal oscillator for connection to 27.12 MHz quartz crystal
- 2.5 V to 3.3 V power supply
- CRC coprocessor
- Programmable I/O pins
- Internal self-test

## 4. Quick reference data

**Table 1. Quick reference data**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V <sub>D<sub>DA</sub></sub>	analog supply voltage	V <sub>DD(PVDD)</sub> ≤ V <sub>D<sub>DA</sub></sub> = V <sub>DD<sub>DD</sub></sub> = V <sub>DD(TVDD)</sub> ;	[1][2]	2.5	3.3	3.6	V
V <sub>D<sub>DD</sub></sub>	digital supply voltage	V <sub>SSA</sub> = V <sub>SSD</sub> = V <sub>SS(PVSS)</sub> = V <sub>SS(TVSS)</sub> = 0 V		2.5	3.3	3.6	V
V <sub>DD(TVDD)</sub>	TVDD supply voltage			2.5	3.3	3.6	V
V <sub>DD(PVDD)</sub>	PVDD supply voltage		[3]	1.6	1.8	3.6	V
V <sub>DD(SVDD)</sub>	SVDD supply voltage	V <sub>SSA</sub> = V <sub>SSD</sub> = V <sub>SS(PVSS)</sub> = V <sub>SS(TVSS)</sub> = 0 V		1.6	-	3.6	V
I <sub>pd</sub>	power-down current	V <sub>D<sub>DA</sub></sub> = V <sub>DD<sub>DD</sub></sub> = V <sub>DD(TVDD)</sub> = V <sub>DD(PVDD)</sub> = 3 V					
		hard power-down; pin NRSTPD set LOW	[4]	-	-	5	μA
		soft power-down; RF level detector on	[4]	-	-	10	μA
I <sub>DD<sub>DD</sub></sub>	digital supply current	pin DVDD; V <sub>D<sub>DD</sub></sub> = 3 V		-	6.5	9	mA
I <sub>DD<sub>DA</sub></sub>	analog supply current	pin AVDD; V <sub>D<sub>DA</sub></sub> = 3 V, CommandReg register's RcvOff bit = 0		-	7	10	mA
		pin AVDD; receiver switched off; V <sub>D<sub>DA</sub></sub> = 3 V, CommandReg register's RcvOff bit = 1		-	3	5	mA
I <sub>DD(PVDD)</sub>	PVDD supply current	pin PVDD	[5]	-	-	40	mA
I <sub>DD(TVDD)</sub>	TVDD supply current	pin TVDD; continuous wave	[6][7][8]	-	60	100	mA
T <sub>amb</sub>	ambient temperature	HVQFN32		-25	-	+85	°C

- [1] Supply voltages below 3 V reduce the performance in, for example, the achievable operating distance.
- [2] V<sub>D<sub>DA</sub></sub>, V<sub>D<sub>DD</sub></sub> and V<sub>DD(TVDD)</sub> must always be the same voltage.
- [3] V<sub>DD(PVDD)</sub> must always be the same or lower voltage than V<sub>D<sub>DD</sub></sub>.
- [4] I<sub>pd</sub> is the total current for all supplies.
- [5] I<sub>DD(PVDD)</sub> depends on the overall load at the digital pins.
- [6] I<sub>DD(TVDD)</sub> depends on V<sub>DD(TVDD)</sub> and the external circuit connected to pins TX1 and TX2.
- [7] During typical circuit operation, the overall current is below 100 mA.
- [8] Typical value using a complementary driver configuration and an antenna matched to 40 Ω between pins TX1 and TX2 at 13.56 MHz.

## 5. Ordering information

Table 2. Ordering information

Type number	Package		Version
	Name	Description	
MF CV52001HN1/TRAYBM <sup>[1]</sup>	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1

[1] Delivered in five trays.

## 6. Block diagram

The analog interface handles the modulation and demodulation of the analog signals.

The contactless UART manages the protocol requirements for the communication protocols in cooperation with the host. The FIFO buffer ensures fast and convenient data transfer to and from the host and the contactless UART and vice versa.

Various host interfaces are implemented to meet different customer requirements.

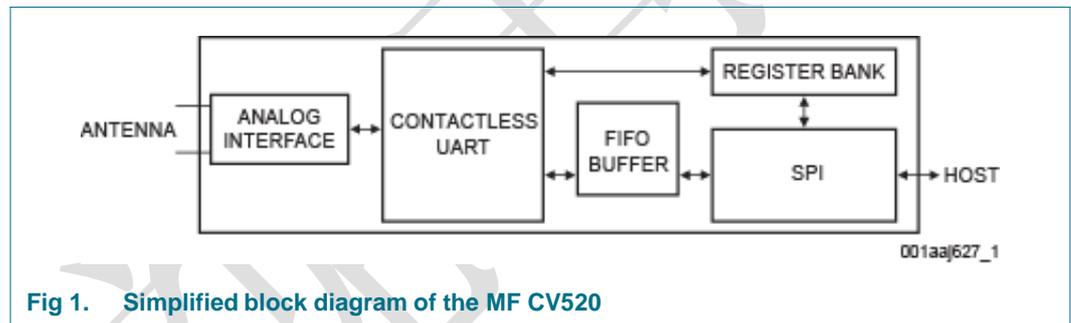


Fig 1. Simplified block diagram of the MF CV520

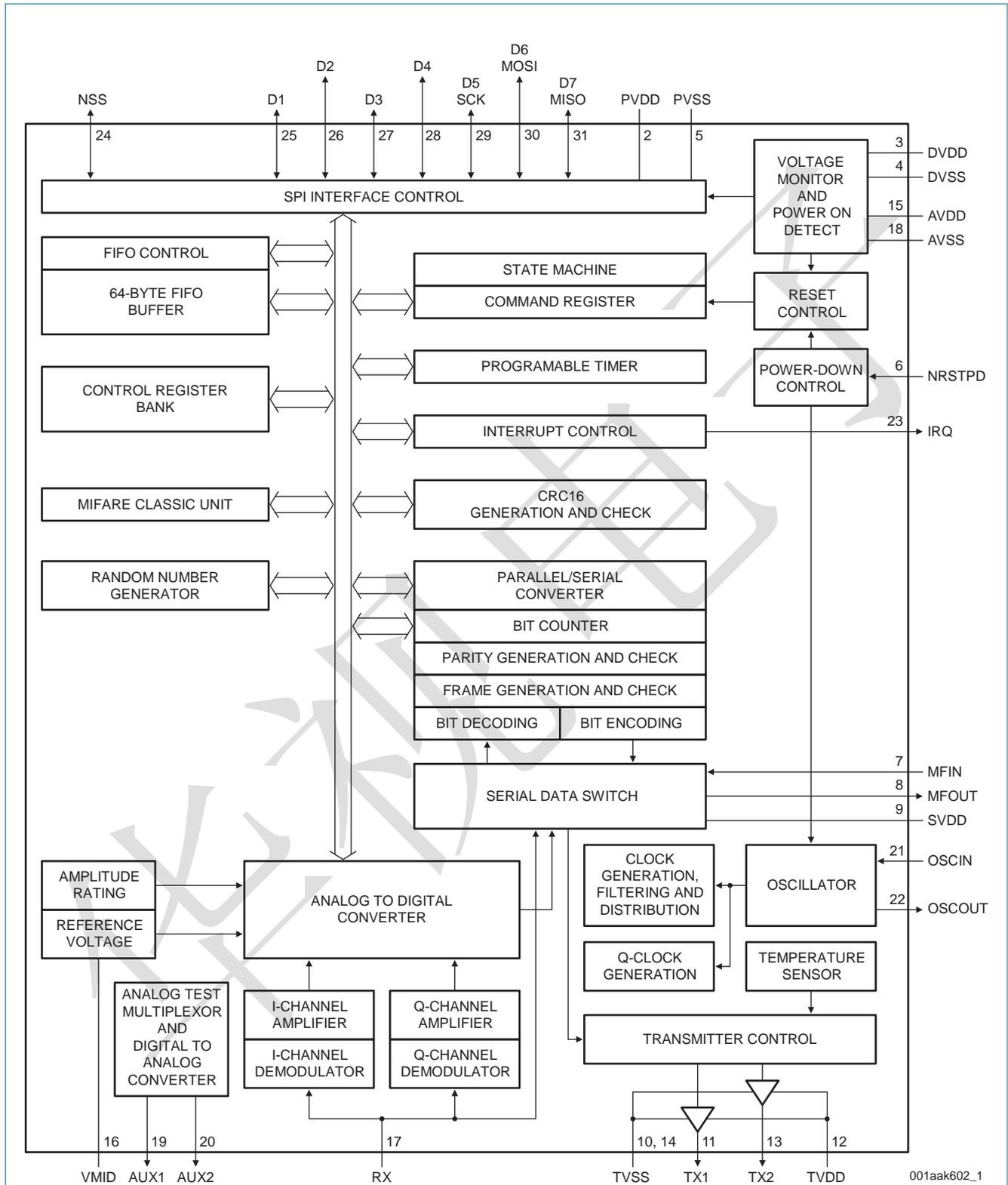


Fig 2. Detailed block diagram of the MF CV520

## 7. Pinning information

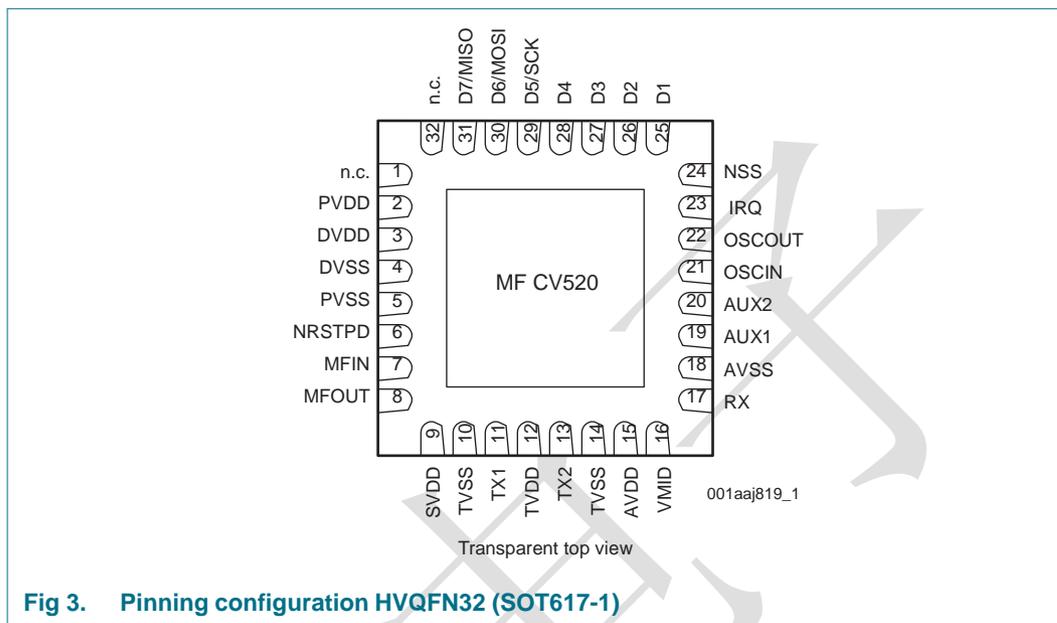


Fig 3. Pinning configuration HVQFN32 (SOT617-1)

### 7.1 Pin description

Table 3. Pin description

Pin	Symbol	Type <sup>[1]</sup>	Description
1	n.c.		not connected
2	PVDD	P	pin power supply
3	DVDD	P	digital power supply
4	DVSS	G	digital ground <sup>[3]</sup>
5	PVSS	G	pin power supply ground
6	NRSTPD	I	reset and power-down input: power-down: enabled when LOW; internal current sinks are switched off, the oscillator is inhibited and the input pins are disconnected from the outside world reset: enabled by a positive edge
7	MFIN	I	MIFARE signal input
8	MFOUT	O	MIFARE signal output
9	SVDD	P	MFIN and MFOUT pin power supply
10	TVSS	G	transmitter output stage 1 ground
11	TX1	O	transmitter 1 modulated 13.56 MHz energy carrier output
12	TVDD	P	transmitter power supply: supplies the output stage of transmitters 1 and 2
13	TX2	O	transmitter 2 modulated 13.56 MHz energy carrier output
14	TVSS	G	transmitter output stage 2 ground
15	AVDD	P	analog power supply
16	VMID	P	internal reference voltage
17	RX	I	RF signal input
18	AVSS	G	analog ground

Table 3. Pin description ...continued

Pin	Symbol	Type <sup>[1]</sup>	Description
19	AUX1	O	auxiliary outputs for test purposes
20	AUX2	O	auxiliary outputs for test purposes
21	OSCIN	I	crystal oscillator inverting amplifier input; also the input for an externally generated clock ( $f_{clk} = 27.12$ MHz)
22	OSCOOUT	O	crystal oscillator inverting amplifier output
23	IRQ	O	interrupt request output: indicates an interrupt event
24	NSS	I	SPI signal input <sup>[2]</sup>
25	D1	I/O	test port <sup>[2]</sup>
26	D2	I/O	test port
27	D3	I/O	test port
28	D4	I/O	test port
29	D5	I/O	test port
	SCK	I	SPI serial clock input <sup>[2]</sup>
30	D6	I/O	test port
	MOSI	I/O	SPI master out, slave in <sup>[2]</sup>
31	D7	I/O	test port
	MISO	I/O	SPI master in, slave out <sup>[2]</sup>
32	n.c.		not connected

[1] Pin types: I = Input, O = Output, I/O = Input/Output, P = Power and G = Ground.

[2] The pin functionality of these pins is explained in [Section 8.1 "Digital interface"](#).

[3] Connection of heatsink pad on package bottom side is not necessary. Optional connection to pin DVSS is possible.

## 8. Functional description

The MF CV520 transmission module supports the Read/Write mode for ISO/IEC 14443 A/MIFARE using various transfer speeds and modulation protocols.

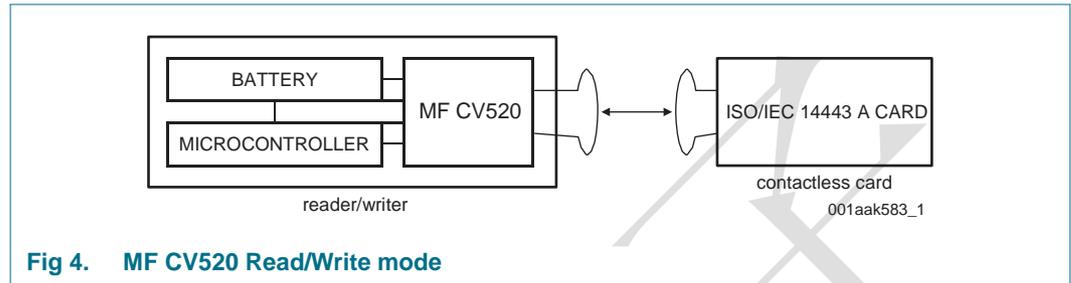


Fig 4. MF CV520 Read/Write mode

The physical level communication is shown in [Figure 5](#).

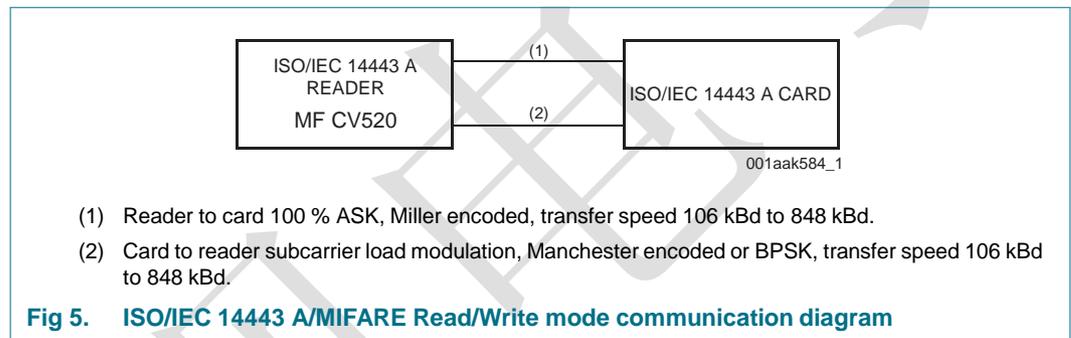


Fig 5. ISO/IEC 14443 A/MIFARE Read/Write mode communication diagram

The physical parameters are described in [Table 4](#).

Table 4. Communication overview for ISO/IEC 14443 A/MIFARE reader/writer

Communication direction	Signal type	Transfer speed			
		106 kBd	212 kBd	424 kBd	848 kBd
Reader to card (send data from the MF CV520 to a card)	reader side modulation	100 % ASK	100 % ASK	100 % ASK	100 % ASK
	bit encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding
	bit length	128 (13.56 μs)	64 (13.56 μs)	32 (13.56 μs)	16 (13.56 μs)
Card to reader (MF CV520 receives data from a card)	card side modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz / 16			
	bit encoding	Manchester encoding	BPSK	BPSK	BPSK

The MF CV520's contactless UART and dedicated external host must manage the complete ISO/IEC 14443 A/MIFARE protocol. [Figure 6](#) shows the data coding and framing according to ISO/IEC 14443 A/MIFARE.

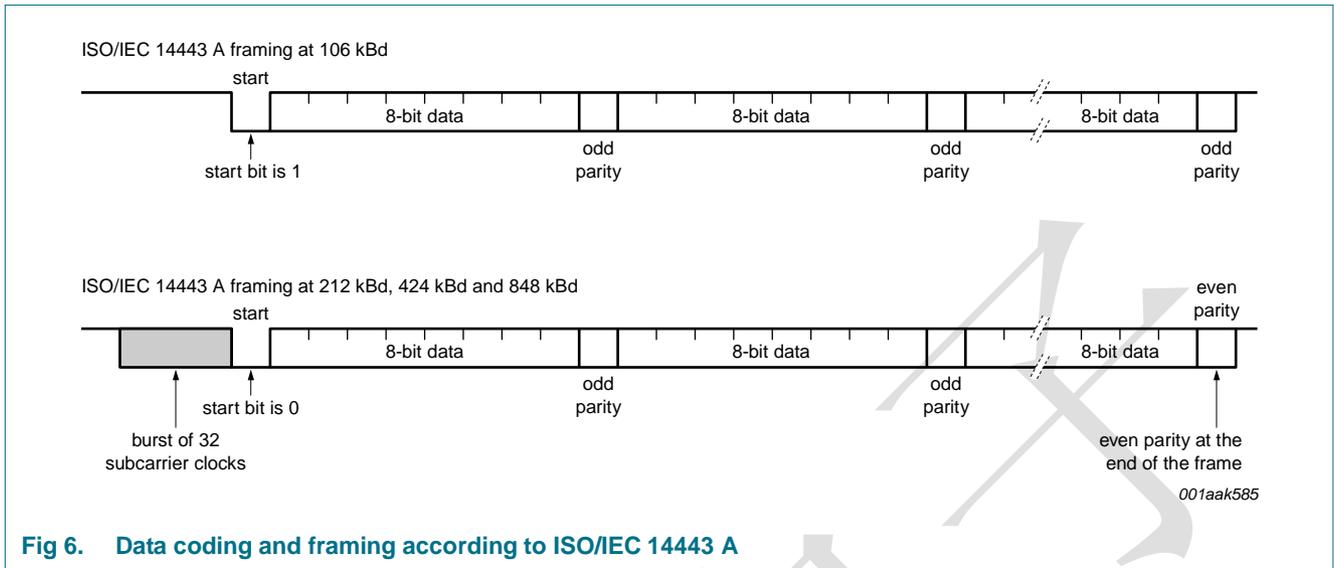


Fig 6. Data coding and framing according to ISO/IEC 14443 A

The internal CRC coprocessor calculates the CRC value based on ISO/IEC 14443 A part 3 and handles parity generation internally according to the transfer speed. Automatic parity generation can be switched off using the MfRxReg register’s ParityDisable bit.

### 8.1 Digital interface

#### 8.1.1 Serial Peripheral Interface

A serial peripheral interface (SPI compatible) is supported to enable high-speed communication to the host. The interface can handle data speeds up to 10 Mbit/s. When communicating with a host, the MF CV520 acts as a slave, receiving data from the external host for register settings, sending and receiving data relevant for RF interface communication.

An interface compatible with SPI enables high-speed serial communication between the MF CV520 and a microcontroller. The implemented interface is in accordance with the SPI standard.

The timing specification is given in [Section 14.1 on page 61](#).

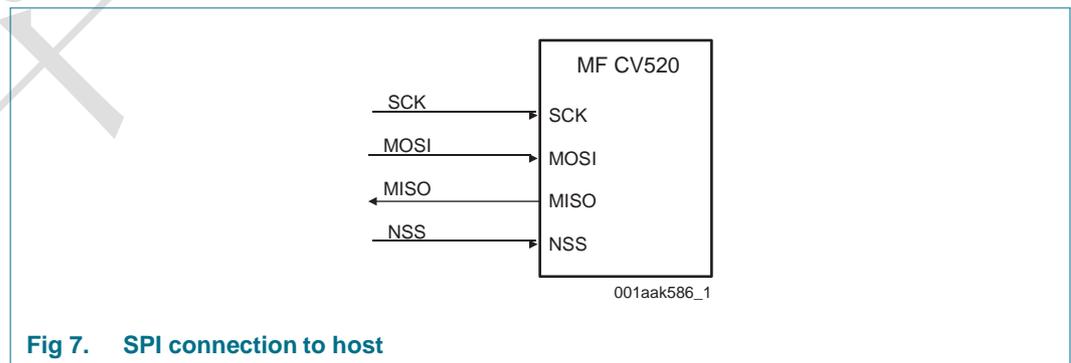


Fig 7. SPI connection to host

The MF CV520 acts as a slave during SPI communication. The SPI clock signal SCK must be generated by the master. Data communication from the master to the slave uses the MOSI line. The MISO line is used to send data from the MF CV520 to the master.

Data bytes on both MOSI and MISO lines are sent with the MSB first. Data on both MOSI and MISO lines must be stable on the rising edge of the clock and can be changed on the falling edge. Data is provided by the MF CV520 on the falling clock edge and is stable during the rising clock edge.

**8.1.1.1 SPI read data**

Reading data using SPI requires the byte order shown in [Table 5](#) to be used. It is possible to read out up to n-data bytes.

The first byte sent defines both the mode and the address.

**Table 5. MOSI and MISO byte order**

Line	Byte 0	Byte 1	Byte 2	To	Byte n	Byte n + 1
MOSI	address 0	address 1	address 2	...	address n	00
MISO	X <sup>[1]</sup>	data 0	data 1	...	data n - 1	data n

[1] X = Do not care.

**Remark:** The MSB must be sent first.

**8.1.1.2 SPI write data**

To write data to the MF CV520 using SPI requires the byte order shown in [Table 6](#). It is possible to write up to n data bytes by only sending one address byte.

The first send byte defines both the mode and the address byte.

**Table 6. MOSI and MISO byte order**

Line	Byte 0	Byte 1	Byte 2	To	Byte n	Byte n + 1
MOSI	address 0	data 0	data 1	...	data n - 1	data n
MISO	X <sup>[1]</sup>	X <sup>[1]</sup>	X <sup>[1]</sup>	...	X <sup>[1]</sup>	X <sup>[1]</sup>

[1] X = Do not care.

**Remark:** The MSB must be sent first.

**8.1.1.3 SPI address byte**

The address byte must meet the following format.

The MSB of the first byte defines the mode used. To read data from the MF CV520 the MSB is set to logic 1. To write data to the MF CV520 the MSB must be set to logic 0. Bits 6 to 1 define the address and the LSB is set to logic 0.

**Table 7. Address byte 0 register; address MOSI**

7 (MSB)	6	5	4	3	2	1	0 (LSB)
1 = read 0 = write	address						0

## 8.2 Analog interface and contactless UART

### 8.2.1 General

The integrated contactless UART supports the external host online with framing and error checking of the protocol requirements up to 848 kBd. An external circuit can be connected to the communication interface pins MFIN and MFOUT to modulate and demodulate the data.

The contactless UART handles the protocol requirements for the communication protocols in cooperation with the host. Protocol handling generates bit and byte-oriented framing. In addition, it handles error detection such as parity and CRC, based on the various supported contactless communication protocols.

**Remark:** The size and tuning of the antenna and the power supply voltage have an important impact on the achievable operating distance.

### 8.2.2 TX p-driver

The signal on pins TX1 and TX2 is the 13.56 MHz energy carrier modulated by an envelope signal. It can be used to drive an antenna directly using a few passive components for matching and filtering; see [Section 15 on page 62](#). The signal on pins TX1 and TX2 can be configured using the TxControlReg register; see [Section 9.3.2.5 on page 34](#).

The modulation index can be set by adjusting the impedance of the drivers. The impedance of the p-driver can be configured using registers CWGsPReg and ModGsPReg. The impedance of the n-driver can be configured using the GsNReg register. The modulation index also depends on the antenna design and tuning.

The TxModeReg and TxSelReg registers control the data rate and framing during transmission and the antenna driver setting to support the different requirements at the different modes and transfer speeds.

**Table 8. Register and bit settings controlling the signal on pin TX1**

Bit Tx1RFEn	Bit Force 100ASK	Bit InvTx1RFOn	Bit InvTx1RFOff	Envelope	Pin TX1	GSPMos	GSNMos	Remarks
0	X <sup>[1]</sup>	not specified if RF is switched off						
1	0	0	X <sup>[1]</sup>	0	RF	pMod	nMod	100 % ASK: pin TX1 pulled to logic 0,
				1	RF	pCW	nCW	
	0	1	X <sup>[1]</sup>	0	RF	pMod	nMod	InvTx1RFOff bit
				1	RF	pCW	nCW	
	1	1	X <sup>[1]</sup>	0	0	pMod	nMod	
				1	RF_n	pCW	nCW	

[1] X = Do not care.

Table 9. Register and bit settings controlling the signal on pin TX2

Bit Tx1RFEn	Bit Force 100ASK	Bit Tx2CW	Bit InvTx2RFOOn	Bit InvTx2RFOff	Envelope	Pin TX2	GSPMos	GSNMos	Remarks		
0	X <sup>[1]</sup>	not specified if RF is switched off									
1	0	0	0	X <sup>[1]</sup>	0	RF	pMod	nMod	-		
					1	RF	pCW	nCW			
			1	X <sup>[1]</sup>	0	RF_n	pMod	nMod			
			1	X <sup>[1]</sup>	1	RF_n	pCW	nCW			
		1	0	X <sup>[1]</sup>	X <sup>[1]</sup>	RF	pCW	nCW	conductance always CW for the Tx2CW bit		
		1		X <sup>[1]</sup>	X <sup>[1]</sup>	RF_n	pCW	nCW			
	1	0	0	0	X <sup>[1]</sup>	0	0	pMod	nMod	100 % ASK: pin TX2 pulled to logic 0 (independent of the InvTx2RFOOn/InvTx2RFOff bits)	
						1	RF	pCW	nCW		
					1	X <sup>[1]</sup>	0	0	pMod		nMod
					1	X <sup>[1]</sup>	1	RF_n	pCW		nCW
	1	0	X <sup>[1]</sup>	X <sup>[1]</sup>	RF	pCW	nCW				
	1		X <sup>[1]</sup>	X <sup>[1]</sup>	RF_n	pCW	nCW				

[1] X = Do not care.

The following abbreviations have been used in [Table 8](#) and [Table 9](#):

- RF: 13.56 MHz clock derived from 27.12 MHz quartz crystal oscillator divided by 2
- RF\_n: inverted 13.56 MHz clock
- GSPMos: conductance, configuration of the PMOS array
- GSNMos: conductance, configuration of the NMOS array
- pCW: PMOS conductance value for continuous wave defined by the CWGsPReg register
- pMod: PMOS conductance value for modulation defined by the ModGsPReg register
- nCW: NMOS conductance value for continuous wave defined by the GsNReg register's CWGsN[3:0] bits
- nMod: NMOS conductance value for modulation defined by the GsNReg register's ModGsN[3:0] bits
- X = do not care.

**Remark:** If only one driver is switched on, the values for CWGsPReg, ModGsPReg and GsNReg registers are used for both drivers.

### 8.2.3 Serial data switch

Two main blocks are implemented in the MF CV520. The digital block comprises the state machines, encoder/decoder logic. The analog block comprises the modulator and antenna drivers, the receiver and amplifiers. It is possible for the interface between these two blocks to be configured so that the interfacing signals are routed to pins MFIN and MFOUT.

This topology allows the analog block of the MF CV520 to be connected to the digital block of another device.

The serial signal switch is controlled by the TxSelReg and RxSelReg registers.

Figure 8 shows the serial data switch for p-driver TX1 and TX2.

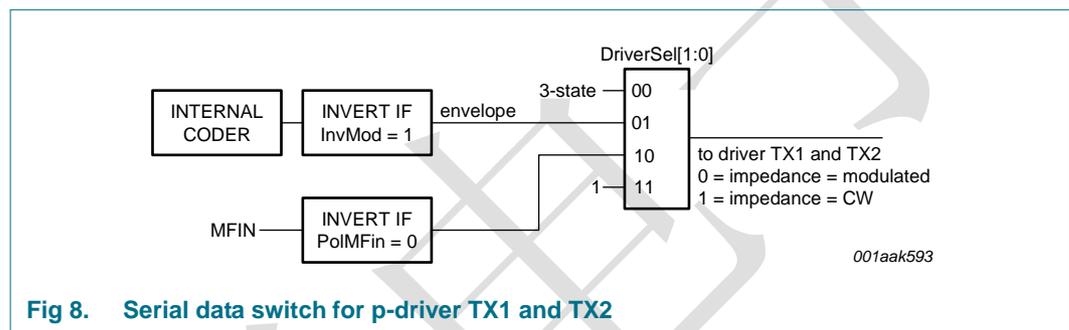


Fig 8. Serial data switch for p-driver TX1 and TX2

### 8.2.4 MFIN and MFOUT interface support

The MF CV520 is divided into a digital circuit block and an analog circuit block. The digital block contains state machines, encoder and decoder logic and so on. The analog block contains the modulator and antenna drivers, receiver and amplifiers. The interface between these two blocks can be configured so that the interfacing signals can be routed to pins MFIN and MFOUT; see Figure 9 on page 13. This configuration is implemented using TxSelReg register's MFOutSel[3:0] and DriverSel[1:0] bits and RxSelReg register's UARTSel[1:0] bits.

This topology allows some parts of the analog block to be connected to the digital block of another device.

Switch MFOutSel in the TxSelReg register can be used to measure MIFARE and ISO/IEC14443 A related signals. This is especially important during the design-in phase or for test purposes as it enables checking of the transmitted and received data.

The most important use of pins MFIN and MFOUT is found in the active antenna concept. An external active antenna circuit can be connected to the MF CV520's digital block. Switch MFOutSel must be configured so that the internal Miller encoded signal is sent to pin MFOUT (MFOutSel = 100b). UARTSel[1:0] must be configured to receive a Manchester signal with subcarrier from pin MFIN (UARTSel[1:0] = 01).

It is possible to connect a passive antenna to pins TX1, TX2 and RX (using the appropriate filter and matching circuit) and an active antenna to pins MFOUT and MFIN at the same time. In this configuration, two RF circuits can be driven (one after another) by a single host processor.

**&Remark:** Pins MFIN and MFOUT have a dedicated supply on pin SVDD with the ground on pin PVSS. If pin MFIN is not used it must be connected to either pin SVDD or pin PVSS. If pin SVDD is not used it must be connected to either pin DVDD, pin PVDD or any other voltage supply pin.

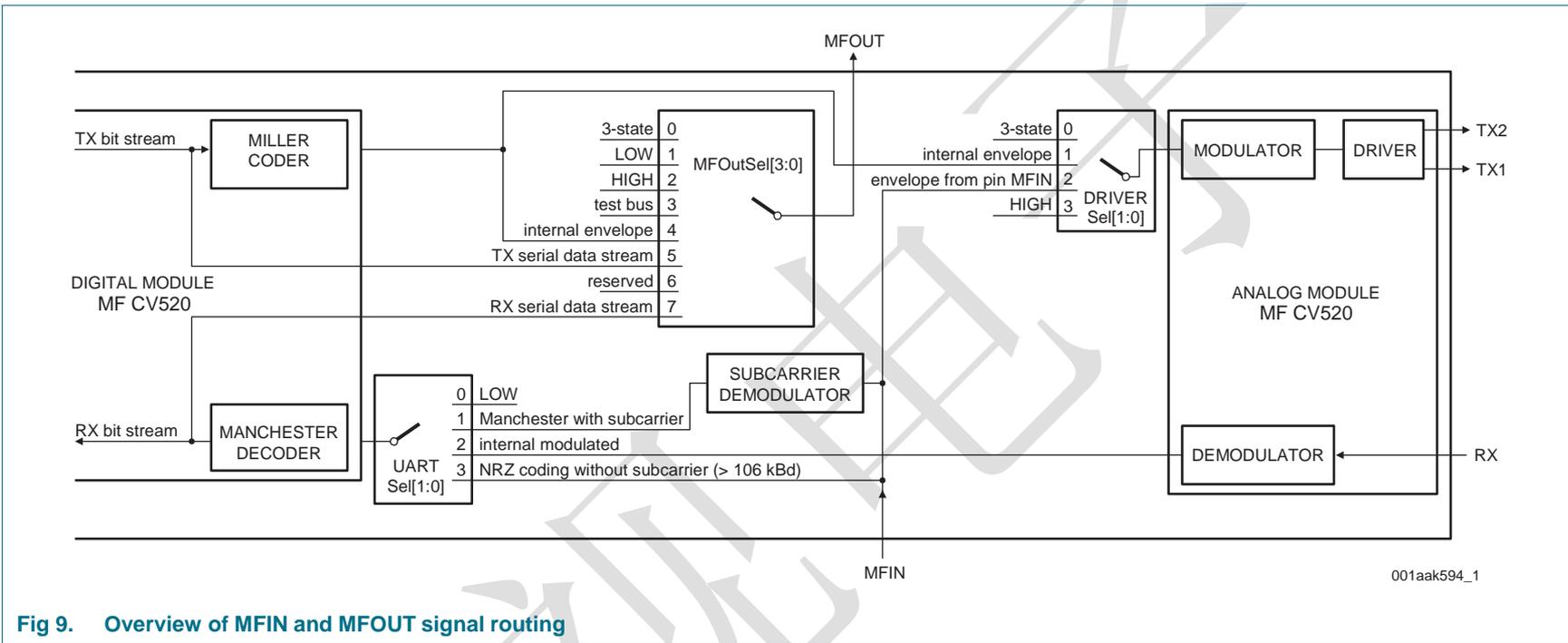


Fig 9. Overview of MFIN and MFOUT signal routing

### 8.2.5 CRC coprocessor

The following CRC coprocessor parameters can be configured:

- The CRC preset value can be either 0000h, 6363h, A671h or FFFFh depending on the ModeReg register's CRCPreset[1:0] bits setting
- The CRC polynomial for the 16-bit CRC is fixed to  $x^{16} + x^{12} + x^5 + 1$
- The CRCResultReg register indicates the result of the CRC calculation. This register is split into two 8-bit registers representing the higher and lower bytes.
- The ModeReg register's MSBFirst bit indicates that data will be loaded with the MSB first.

**Table 10. CRC coprocessor parameters**

Parameter	Value
CRC register length	16-bit CRC
CRC algorithm	algorithm according to ISO/IEC 14443 A and ITU-T
CRC preset value	0000h, 6363h, A671h or FFFFh depending on the setting of the ModeReg register's CRCPreset[1:0] bits

## 8.3 FIFO buffer

An 8 × 64 bit FIFO buffer is used in the MF CV520. It buffers the input and output data stream between the host and the MF CV520's internal state machine. This makes it possible to manage data streams up to 64 bytes long without the need to take timing constraints into account.

### 8.3.1 Accessing the FIFO buffer

The FIFO buffer input and output data bus is connected to the FIFODataReg register. Writing to this register stores one byte in the FIFO buffer and increments the internal FIFO buffer write pointer. Reading from this register shows the FIFO buffer contents stored in the FIFO buffer read pointer and decrements the FIFO buffer read pointer. The distance between the write and read pointer can be obtained by reading the FIFOLevelReg register.

When the microcontroller starts a command, the MF CV520 can, while the command is in progress, access the FIFO buffer according to that command. Only one FIFO buffer has been implemented which can be used for input and output. The microcontroller must ensure that there are not any unintentional FIFO buffer accesses.

### 8.3.2 Controlling the FIFO buffer

The FIFO buffer pointers can be reset by setting FIFOLevelReg register's FlushBuffer bit to logic 1. Consequently, the FIFOLevel[6:0] bits are all set to logic 0 and the ErrorReg register's BufferOvfl bit is cleared. The bytes stored in the FIFO buffer are no longer accessible allowing the FIFO buffer to be filled with another 64 bytes.

### 8.3.3 FIFO buffer status information

The host can get the following FIFO buffer status information:

- Number of bytes stored in the FIFO buffer: FIFOLevelReg register's FIFOLevel[6:0]
- FIFO buffer almost full warning: Status1Reg register's HiAlert bit

- FIFO buffer almost empty warning: Status1Reg register's LoAlert bit
- FIFO buffer overflow warning: ErrorReg register's BufferOvfl bit. The BufferOvfl bit can only be cleared by setting the FIFOLevelReg register's FlushBuffer bit.

The MF CV520 can generate an interrupt signal when:

- ComIEnReg register's LoAlertIEn bit is set to logic 1. It activates pin IRQ when Status1Reg register's LoAlert bit changes to logic 1.
- ComIEnReg register's HiAlertIEn bit is set to logic 1. It activates pin IRQ when Status1Reg register's HiAlert bit changes to logic 1.

If the maximum number of WaterLevel bytes (as set in the WaterLevelReg register) or less are stored in the FIFO buffer, the HiAlert bit is set to logic 1. It is generated according to [Equation 1](#):

$$HiAlert = (64 - FIFOLength) \leq WaterLevel \quad (1)$$

If the number of WaterLevel bytes (as set in the WaterLevelReg register) or less are stored in the FIFO buffer, the LoAlert bit is set to logic 1. It is generated according to [Equation 2](#):

$$LoAlert = FIFOLength \leq WaterLevel \quad (2)$$

## 8.4 Interrupt request system

The MF CV520 indicates certain events by setting the Status1Reg register's IRq bit and, if activated, by pin IRQ. The signal on pin IRQ can be used to interrupt the host using its interrupt handling capabilities. This allows the implementation of efficient host software.

### 8.4.1 Interrupt sources overview

[Table 11](#) shows the available interrupt bits, the corresponding source and the condition for its activation. The ComIrqReg register's TimerIRq interrupt bit indicates an interrupt set by the timer unit which is set when the timer decrements from 1 to 0.

The ComIrqReg register's TxIRq bit indicates that the transmitter has finished. If the state changes from sending data to transmitting the end of the frame pattern, the transmitter unit automatically sets the interrupt bit. The CRC coprocessor sets the DivIrqReg register's CRCIRq bit after processing all the FIFO buffer data which is indicated by CRCReady bit = 1.

The ComIrqReg register's RxIRq bit indicates an interrupt when the end of the received data is detected. The ComIrqReg register's IdleIRq bit is set if a command finishes and the Command[3:0] value in the CommandReg register changes to idle (see [Table 140 on page 53](#)).

The ComIrqReg register's HiAlertIRq bit is set to logic 1 when the Status1Reg register's HiAlert bit is set to logic 1 which means that the FIFO buffer has reached the level indicated by the WaterLevel[5:0] bits.

The ComIrqReg register's LoAlertIRq bit is set to logic 1 when the Status1Reg register's LoAlert bit is set to logic 1 which means that the FIFO buffer has reached the level indicated by the WaterLevel[5:0] bits.

The ComIrqReg register's ErrIRq bit indicates an error detected by the contactless UART during send or receive. This is indicated when any bit is set to logic 1 in register ErrorReg.

**Table 11. Interrupt sources**

Interrupt flag	Interrupt source	Trigger action
IRq	timer unit	the timer counts from 1 to 0
TxIRq	transmitter	a transmitted data stream ends
CRCIRq	CRC coprocessor	all data from the FIFO buffer has been processed
RxIRq	receiver	a received data stream ends
IdleIRq	ComIrqReg register	command execution finishes
HiAlertIRq	FIFO buffer	the FIFO buffer is almost full
LoAlertIRq	FIFO buffer	the FIFO buffer is almost empty
ErrIRq	contactless UART	an error is detected

## 8.5 Timer unit

The MF CV520A has a timer unit which the external host can use to manage timing tasks. The timer unit can be used in one of the following timer/counter configurations:

- Timeout counter
- Watchdog counter
- Stop watch
- Programmable one shot
- Periodical trigger

The timer unit can be used to measure the time interval between two events or to indicate that a specific event occurred after a specific time. The timer can be triggered by events explained in the paragraphs below. The timer does not influence any internal events, for example, a time-out during data reception does not automatically influence the reception process. Furthermore, several timer-related bits can be used to generate an interrupt.

The timer has an input clock of 13.56 MHz derived from the 27.12 MHz quartz crystal oscillator. The timer consists of two stages: prescaler and counter.

The prescaler (TPrescaler) is a 12-bit counter. The reload values (TReloadVal\_Hi[7:0] and TReloadVal\_Lo[7:0]) for TPrescaler can be set between 0 and 4095 in the TModeReg register's TPrescaler\_Hi[3:0] bits and TPrescalerReg register's TPrescaler\_Lo[7:0] bits.

The reload value for the counter is defined by 16 bits between 0 and 65535 in the TReloadReg register.

The current value of the timer is indicated in the TCounterValReg register.

When the counter reaches 0, an interrupt is automatically generated, indicated by the ComIrqReg register's TimerIRq bit setting. If enabled, this event can be indicated on pin IRQ. The TimerIRq bit can be set and reset by the host. Depending on the configuration, the timer will stop at 0 or restart with the value set in the TReloadReg register.

The timer status is indicated by the Status1Reg register's TRunning bit.

The timer can be started manually using the ControlReg register's TStartNow bit and stopped using the ControlReg register's TStopNow bit.

The timer can also be activated automatically to meet any dedicated protocol requirements by setting the TModeReg register's TAuto bit to logic 1.

The delay time of a timer stage is set by the reload value + 1. The total delay time ( $t_d$ ) is calculated using [Equation 3](#):

$$t_d = \frac{(TPrescaler \times 2 + 1) \times (TReloadVal + 1)}{13,56 \text{ MHz}} \quad (3)$$

An example of calculating total delay time ( $t_d$ ) is shown in [Equation 4](#), where the TPrescaler value = 4095 and TReloadVal = 65535:

$$39,59 \text{ s} = \frac{(4095 \times 2 + 1) \times (65535 + 1)}{13,56 \text{ MHz}} \quad (4)$$

**Example:** To give a delay time of 25  $\mu$ s requires 339 clock cycles to be counted and a TPrescaler value of 169. This configures the timer to count up to 65535 time-slots for every 25  $\mu$ s period.

## 8.6 Power reduction modes

### 8.6.1 Hard power-down

Hard power-down is enabled when pin NRSTPD is LOW. This turns off all internal current sinks including the oscillator. All digital input buffers are separated from the input pins and clamped internally (except pin NRSTPD). The output pins are frozen at either a HIGH or LOW level.

### 8.6.2 Soft power-down mode

Soft Power-down mode is entered immediately after the CommandReg register's PowerDown bit is set to logic 1. All internal current sinks are switched off, including the oscillator buffer. However, the digital input buffers are not separated from the input pins and keep their functionality. The digital output pins do not change their state.

During soft power-down, all register values, the FIFO buffer content and the configuration keep their current contents.

After setting the PowerDown bit to logic 0, it takes 1024 clocks until the Soft power-down mode is exited indicated by the PowerDown bit. Setting it to logic 0 does not immediately clear it. It is cleared automatically by the MF CV520 when Soft power-down mode is exited.

**Remark:** If the internal oscillator is used, you must take into account that it is supplied by pin AVDD and it will take a certain time ( $t_{osc}$ ) until the oscillator is stable and the clock cycles can be detected by the internal logic. It is recommended for the serial UART, to first send the value 55h to the MF CV520. The oscillator must be stable for further access to the registers. To ensure this, perform a read access to address 0 until the MF CV520 answers to the last read command with the register content of address 0. This indicates that the MF CV520 is ready.

### 8.6.3 Transmitter power-down mode

The Transmitter Power-down mode switches off the internal antenna drivers thereby, turning off the RF field. Transmitter power-down mode is entered by setting either the TxControlReg register's Tx1RFEn bit or Tx2RFEn bit to logic 0.

## 8.7 Oscillator circuit

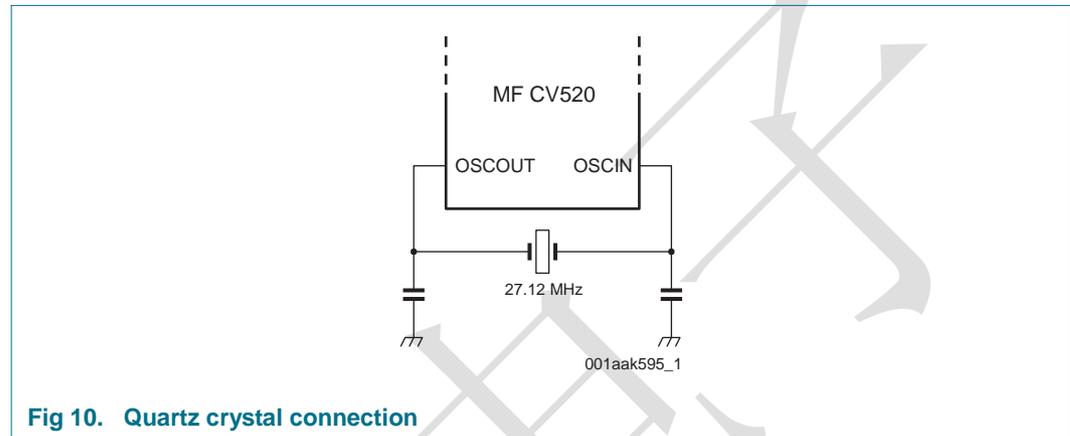


Fig 10. Quartz crystal connection

The clock applied to the MF CV520 provides a time basis for the synchronous system's encoder and decoder. The stability of the clock frequency, therefore, is an important factor for correct operation. To obtain optimum performance, clock jitter must be reduced as much as possible. This is best achieved using the internal oscillator buffer with the recommended circuitry.

If an external clock source is used, the clock signal must be applied to pin OSCIN. In this case, special care must be taken with the clock duty cycle and clock jitter and the clock quality must be verified.

## 8.8 Reset and oscillator start-up time

### 8.8.1 Reset timing requirements

The reset signal is filtered by a hysteresis circuit and a spike filter before it enters the digital circuit. The spike filter rejects signals shorter than 10 ns. In order to perform a reset, the signal must be LOW for at least 100 ns.

### 8.8.2 Oscillator start-up time

If the MF CV520 has been set to a Power-down mode or is powered by a  $V_{DDX}$  supply, the start-up time for the MF CV520 depends on the oscillator used and is shown in [Figure 11](#).

The time ( $t_{startup}$ ) is the start-up time of the crystal oscillator circuit. The crystal oscillator start-up time is defined by the crystal.

The time ( $t_d$ ) is the internal delay time of the MF CV520 when the clock signal is stable before the MF CV520 can be addressed.

The delay time is calculated by:

$$t_d = \frac{1024}{27 \mu\text{s}} = 37,74 \mu\text{s} \quad (5)$$

The time ( $t_{\text{osc}}$ ) is the sum of  $t_d$  and  $t_{\text{startup}}$ .

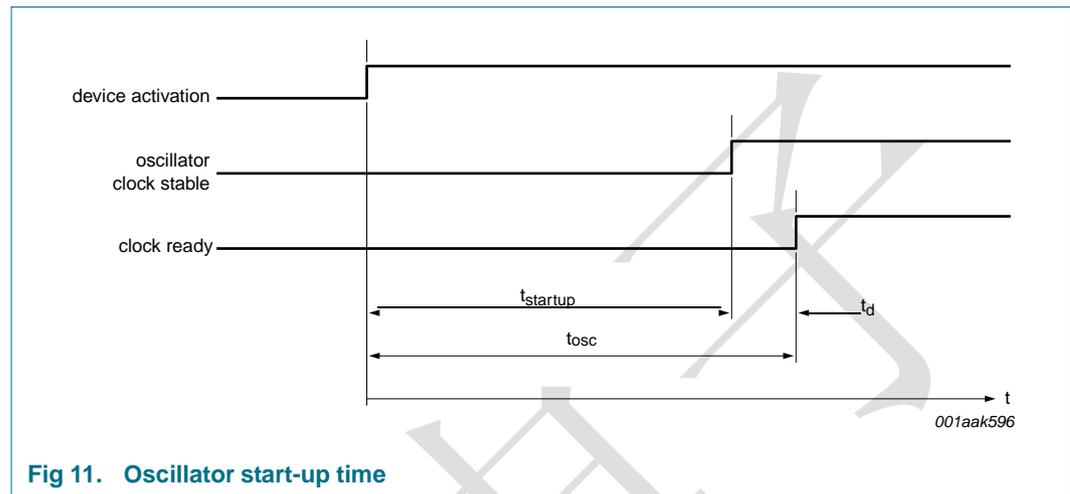


Fig 11. Oscillator start-up time

## 9. MF CV520 registers

### 9.1 Register bit behavior

Depending on the functionality of a register, the access conditions to the register can vary. In principle, bits with same behavior are grouped in common registers. The access conditions are described in [Table 12](#).

Table 12. Behavior of register bits and their designation

Abbreviation	Behavior	Description
R/W	read and write	These bits can be written and read by the microcontroller. Since they are used only for control purposes, their content is not influenced by internal state machines, for example the ComIEnReg register can be written and read by the microcontroller. It will also be read by internal state machines but never changed by them.
D	dynamic	These bits can be written and read by the microcontroller. Nevertheless, they can also be written automatically by internal state machines, for example the CommandReg register changes its value automatically after the execution of the command.
R	read only	These register bits hold values which are determined by internal states only, for example the CRCReady bit cannot be written externally but shows internal states.
W	write only	Reading these register bits always returns zero.
reserved	-	These registers are reserved for future use and must not be changed. In case of a write access, it is recommended to always write the value "0".
RFT	-	These register bits are reserved for future use or are for production tests and must not be changed.

## 9.2 Register overview

**Table 13. MF CV520 register overview**

Address (hex)	Register name	Function	Refer to
<b>Page 0: Command and status</b>			
00h	Reserved	reserved for future use	<a href="#">Table 14 on page 22</a>
01h	CommandReg	starts and stops command execution	<a href="#">Table 16 on page 22</a>
02h	ComlEnReg	enable and disable interrupt request control bits	<a href="#">Table 18 on page 22</a>
03h	DivlEnReg	enable and disable interrupt request control bits	<a href="#">Table 20 on page 23</a>
04h	ComlRqReg	interrupt request bits	<a href="#">Table 22 on page 23</a>
05h	DivlRqReg	interrupt request bits	<a href="#">Table 24 on page 24</a>
06h	ErrorReg	error bits showing the error status of the last command executed	<a href="#">Table 26 on page 25</a>
07h	Status1Reg	communication status bits	<a href="#">Table 28 on page 26</a>
08h	Status2Reg	receiver and transmitter status bits	<a href="#">Table 30 on page 27</a>
09h	FIFODataReg	input and output of 64 byte FIFO buffer	<a href="#">Table 32 on page 28</a>
0Ah	FIFOLevelReg	number of bytes stored in the FIFO buffer	<a href="#">Table 34 on page 28</a>
0Bh	WaterLevelReg	level for FIFO underflow and overflow warning	<a href="#">Table 36 on page 28</a>
0Ch	ControlReg	miscellaneous control registers	<a href="#">Table 38 on page 29</a>
0Dh	BitFramingReg	adjustments for bit-oriented frames	<a href="#">Table 40 on page 30</a>
0Eh	CollReg	bit position of the first bit-collision detected on the RF interface	<a href="#">Table 42 on page 30</a>
0Fh	Reserved	reserved for future use	<a href="#">Table 44 on page 31</a>
<b>Page 1: Command</b>			
10h	Reserved	reserved for future use	<a href="#">Table 46 on page 31</a>
11h	ModeReg	defines general modes for transmitting and receiving	<a href="#">Table 48 on page 32</a>
12h	TxModeReg	defines transmission data rate and framing	<a href="#">Table 50 on page 32</a>
13h	RxModeReg	defines reception data rate and framing	<a href="#">Table 52 on page 33</a>
14h	TxControlReg	controls the logical behavior of the antenna driver pins TX1 and TX2	<a href="#">Table 54 on page 34</a>
15h	TxASKReg	controls the setting of the transmission modulation	<a href="#">Table 56 on page 35</a>
16h	TxSelReg	selects the internal sources for the antenna driver	<a href="#">Table 58 on page 35</a>
17h	RxSelReg	selects internal receiver settings	<a href="#">Table 60 on page 36</a>
18h	RxThresholdReg	selects thresholds for the bit decoder	<a href="#">Table 62 on page 37</a>
19h	DemodReg	defines demodulator settings	<a href="#">Table 64 on page 37</a>
1Ah	Reserved	reserved for future use	<a href="#">Table 66 on page 38</a>
1Bh	Reserved	reserved for future use	<a href="#">Table 68 on page 38</a>
1Ch	MfTxReg	controls some MIFARE communication transmit parameters	<a href="#">Table 70 on page 38</a>
1Dh	MfRxReg	controls some MIFARE communication receive parameters	<a href="#">Table 72 on page 39</a>
1Eh	Reserved	reserved for future use	<a href="#">Table 74 on page 39</a>
1Fh	Reserved	reserved for future use	<a href="#">Table 74 on page 39</a>
<b>Page 2: Configuration</b>			
20h	Reserved	reserved for future use	<a href="#">Table 76 on page 40</a>

**Table 13. MF CV520 register overview ...continued**

Address (hex)	Register name	Function	Refer to
21h	CRCResultReg	shows the MSB and LSB values of the CRC calculation	<a href="#">Table 78 on page 40</a>
22h			<a href="#">Table 80 on page 40</a>
23h	Reserved	reserved for future use	<a href="#">Table 82 on page 41</a>
24h	ModWidthReg	controls the ModWidth setting	<a href="#">Table 84 on page 41</a>
25h	Reserved	reserved for future use	<a href="#">Table 86 on page 41</a>
26h	RFCfgReg	configures the receiver gain	<a href="#">Table 88 on page 42</a>
27h	GsNReg	selects the conductance of the antenna driver pins TX1 and TX2 for modulation	<a href="#">Table 90 on page 42</a>
28h	CWGsPReg	defines the conductance of the p-driver output during periods of no modulation	<a href="#">Table 92 on page 43</a>
29h	ModGsPReg	defines the conductance of the p-driver output during periods of modulation	<a href="#">Table 94 on page 43</a>
2Ah	TModeReg	defines settings for the internal timer	<a href="#">Table 96 on page 43</a>
2Bh	TPrescalerReg		<a href="#">Table 98 on page 44</a>
2Ch	TReloadReg	defines the 16-bit timer reload value	<a href="#">Table 100 on page 45</a>
2Dh			<a href="#">Table 102 on page 45</a>
2Eh	TCounterValReg	shows the 16-bit timer value	<a href="#">Table 104 on page 46</a>
2Fh			<a href="#">Table 106 on page 46</a>
<b>Page 3: Test register</b>			
30h	Reserved	reserved for future use	<a href="#">Table 108 on page 46</a>
31h	TestSel1Reg	general test signal configuration	<a href="#">Table 110 on page 46</a>
32h	TestSel2Reg	general test signal configuration and PRBS control	<a href="#">Table 112 on page 47</a>
33h	TestPinEnReg	enables pin output driver on pins D1 to D7	<a href="#">Table 114 on page 47</a>
34h	TestPinValueReg	defines the values for D1 to D7 when it is used as an I/O bus	<a href="#">Table 116 on page 48</a>
35h	TestBusReg	shows the status of the internal test bus	<a href="#">Table 118 on page 48</a>
36h	AutoTestReg	controls the digital self test	<a href="#">Table 120 on page 49</a>
37h	VersionReg	shows the software version	<a href="#">Table 122 on page 49</a>
38h	AnalogTestReg	controls the pins AUX1 and AUX2	<a href="#">Table 124 on page 50</a>
39h	TestDAC1Reg	defines the test value for TestDAC1	<a href="#">Table 126 on page 51</a>
3Ah	TestDAC2Reg	defines the test value for TestDAC2	<a href="#">Table 128 on page 51</a>
3Bh	TestADCReg	shows the value of ADC I and Q channels	<a href="#">Table 130 on page 51</a>
3Ch to 3Fh	Reserved	reserved for production tests	<a href="#">Table 132 to Table 138 on page 52</a>

## 9.3 Register descriptions

### 9.3.1 Page 0: Command and status

#### 9.3.1.1 Reserved register 00h

Functionality is reserved for future use.

**Table 14. Reserved register (address 00h); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

**Table 15. Reserved register bit descriptions**

Bit	Symbol	Description
7 to 0	-	reserved

#### 9.3.1.2 CommandReg register

Starts and stops command execution.

**Table 16. CommandReg register (address 01h); reset value: 20h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol:	reserved		RcvOff	PowerDown		Command[3:0]		
Access:		-	R/W	D		D		

**Table 17. CommandReg register bit descriptions**

Bit	Symbol	Value	Description
7 to 6	reserved	-	reserved for future use
5	RcvOff	1	analog part of the receiver is switched off
4	PowerDown	1	Soft power-down mode entered
		0	MF CV520 starts the wake up procedure during which this bit is read as a logic 1; it is read as a logic 0 when the MF CV520 is ready; see <a href="#">Section 8.6.2 on page 17</a>
			<b>Remark:</b> The PowerDown bit cannot be set when the SoftReset command is activated
3 to 0	Command[3:0]	-	activates a command based on the Command value; reading this register shows which command is executed; see <a href="#">Section 10.3 on page 53</a>

#### 9.3.1.3 ComIEnReg register

Control bits to enable and disable the passing of interrupt requests.

**Table 18. ComIEnReg register (address 02h); reset value: 80h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	IRqInv	TxIEn	RxIEn	IdleIEn	HiAlertIEn	LoAlertIEn	ErrIEn	TimerIEn
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 19. ComlEnReg register bit descriptions**

Bit	Symbol	Value	Description
7	IRqInv	1	signal on pin IRQ is inverted with respect to the Status1Reg register's IRq bit
		0	signal on pin IRQ is equal to the IRq bit; in combination with the DivlEnReg register's IRqPushPull bit, the default value of logic 1 ensures that the output level on pin IRQ is 3-state
6	TxlEn	-	allows the transmitter interrupt request (TxIRq bit) to be propagated to pin IRQ
5	RxlEn	-	allows the receiver interrupt request (RxIRq bit) to be propagated to pin IRQ
4	IdlelEn	-	allows the idle interrupt request (IdleIRq bit) to be propagated to pin IRQ
3	HiAlertlEn	-	allows the high alert interrupt request (HiAlertIRq bit) to be propagated to pin IRQ
2	LoAlertlEn	-	allows the low alert interrupt request (LoAlertIRq bit) to be propagated to pin IRQ
1	ErrlEn	-	allows the error interrupt request (ErrIRq bit) to be propagated to pin IRQ
0	TimerlEn	-	allows the timer interrupt request (TimerIRq bit) to be propagated to pin IRQ

#### 9.3.1.4 DivlEnReg register

Control bits to enable and disable the passing of interrupt requests.

**Table 20. DivlEnReg register (address 03h); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	IRQPushPull	reserved	MfinActlEn	reserved	CRCIEEn	reserved		
Access	R/W	-	R/W	-	R/W	-		

**Table 21. DivlEnReg register bit descriptions**

Bit	Symbol	Value	Description
7	IRQPushPull	1	pin IRQ is a standard CMOS output pin
		0	pin IRQ is an open-drain output pin
6 to 5	reserved	-	reserved for future use
4	MfinActlEn	-	allows the MFIN active interrupt request to be propagated to pin IRQ
3	reserved	-	reserved for future use
2	CRCIEEn	-	allows the CRC interrupt request, indicated by the DivlRqReg register's CRCIRq bit, to be propagated to pin IRQ
1 to 0	reserved	-	reserved for future use

#### 9.3.1.5 ComlRqReg register

Interrupt request bits.

**Table 22. ComlRqReg register (address 04h); reset value: 14h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	Set1	TxlRq	RxlRq	IdleIRq	HiAlertIRq	LoAlertIRq	ErrIRq	TimerIRq
Access	W	D	D	D	D	D	D	D

**Table 23. ComlRqReg register bit descriptions**

All bits in the ComlRqReg register are cleared by software.

Bit	Symbol	Value	Description
7	Set1	1	indicates that the marked bits in the ComlRqReg register are set
		0	indicates that the marked bits in the ComlRqReg register are cleared
6	TxIRq	1	set immediately after the last bit of the transmitted data was sent out
5	RxIRq	1	receiver has detected the end of a valid data stream if the RxModeReg register's RxNoErr bit is set to logic 1, the RxIRq bit is only set to logic 1 when data bytes are available in the FIFO
4	IdleIRq	1	If a command terminates, for example, when the CommandReg changes its value from any command to the Idle command (see <a href="#">Table 140 on page 53</a> ) if an unknown command is started, the CommandReg register Command[3:0] value changes to the idle state and the IdleIRq bit is set The microcontroller starting the Idle command does not set the IdleIRq bit
3	HiAlertIRq	1	the Status1Reg register's HiAlert bit is set in opposition to the HiAlert bit, the HiAlertIRq bit stores this event and can only be reset as indicated by the Set1 bit in this register
2	LoAlertIRq	1	Status1Reg register's LoAlert bit is set in opposition to the LoAlert bit, the LoAlertIRq bit stores this event and can only be reset as indicated by the Set1 bit in this register
1	ErrIRq	1	any error bit in the ErrorReg register is set
0	TimerIRq	1	the timer decrements the timer value in register TCounterValReg to zero

### 9.3.1.6 DivlRqReg register

Interrupt request bits.

**Table 24. DivlRqReg register (address 05h); reset value: x0h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	Set2	reserved		MfinActIRq	reserved	CRCIRq		reserved
Access	W	-		D	-	D		-

**Table 25. DivlRqReg register bit descriptions**

All bits in the DivlRqReg register are cleared by software.

Bit	Symbol	Value	Description
7	Set2	1	indicates that the marked bits in the DivlRqReg register are set
		0	indicates that the marked bits in the DivlRqReg register are cleared
6 to 5	reserved	-	reserved for future use
4	MfinActIRq	1	MFIN is active this interrupt is set when either a rising or falling signal edge is detected
3	reserved	-	reserved for future use
2	CRCIRq	1	the CalcCRC command is active and all data is processed
1 to 0	reserved	-	reserved for future use

### 9.3.1.7 ErrorReg register

Error bit register showing the error status of the last command executed.

**Table 26. ErrorReg register (address 06h); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	WrErr	TempErr	reserved	BufferOvfl	CollErr	CRCErr	ParityErr	ProtocolErr
Access	R	R	-	R	R	R	R	R

**Table 27. ErrorReg register bit descriptions**

Bit	Symbol	Value	Description
7	WrErr	1	data is written into the FIFO buffer by the host during the MFAuthent command or if data is written into the FIFO buffer by the host during the time between sending the last bit on the RF interface and receiving the last bit on the RF interface
6	TempErr <sup>[1]</sup>	1	internal temperature sensor detects overheating, in which case the antenna drivers are automatically switched off
5	reserved	-	reserved for future use
4	BufferOvfl	1	the host or a MF CV520's internal state machine (e.g. receiver) tries to write data to the FIFO buffer even though it is already full
3	CollErr	1	a bit-collision is detected cleared automatically at receiver start-up phase only valid during the bitwise anticollision at 106 kBd always set to logic 0 during communication protocols at 212 kBd, 424 kBd and 848 kBd
2	CRCErr	1	the RxModeReg register's RxCRCEn bit is set and the CRC calculation fails automatically cleared to logic 0 during receiver start-up phase
1	ParityErr	1	parity check failed automatically cleared during receiver start-up phase only valid for ISO/IEC 14443 A/MIFARE communication at 106 kBd
0	ProtocolErr	1	set to logic 1 if the SOF is incorrect automatically cleared during receiver start-up phase bit is only valid for 106 kBd during the MFAuthent command, the ProtocolErr bit is set to logic 1 if the number of bytes received in one data stream is incorrect

[1] Command execution clears all error bits except the TempErr bit. Cannot be set by software.

### 9.3.1.8 Status1Reg register

Contains status bits of the CRC, interrupt and FIFO buffer.

**Table 28. Status1Reg register (address 07h); reset value: 21h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	CRCOk	CRCReady	IRq	TRunning	reserved	HiAlert	LoAlert
Access	-	R	R	R	R	-	R	R

**Table 29. Status1Reg register bit descriptions**

Bit	Symbol	Value	Description
7	reserved	-	reserved for future use
6	CRCOk	1	the CRC result is zero for data transmission and reception, the CRCOk bit is undefined: use the ErrorReg register's CRCErr bit indicates the status of the CRC coprocessor, during calculation the value changes to logic 0, when the calculation is done correctly the value changes to logic 1
5	CRCReady	1	the CRC calculation has finished only valid for the CRC coprocessor calculation using the CalcCRC command
4	IRq	-	indicates if any interrupt source requests attention with respect to the setting of the interrupt enable bits: see the ComIEnReg and DivIEnReg registers
3	TRunning	1	MF CV520's timer unit is running, i.e. the timer will decrement the TCounterValReg register with the next timer clock <b>Remark:</b> in gated mode, the TRunning bit is set to logic 1 when the timer is enabled by TModeReg register's TGated[1:0] bits; this bit is not influenced by the gated signal
2	reserved	-	reserved for future use
1	HiAlert	1	the number of bytes stored in the FIFO buffer corresponds to equation: $HiAlert = (64 - FIFOLength) \leq WaterLevel$ example: FIFO length = 60, WaterLevel = 4 → HiAlert = 1 FIFO length = 59, WaterLevel = 4 → HiAlert = 0
0	LoAlert	1	the number of bytes stored in the FIFO buffer corresponds to equation: $LoAlert = FIFOLength \leq WaterLevel$ example: FIFO length = 4, WaterLevel = 4 → LoAlert = 1 FIFO length = 5, WaterLevel = 4 → LoAlert = 0

### 9.3.1.9 Status2Reg register

Contains status bits of the receiver, transmitter and data mode detector.

**Table 30. Status2Reg register (address 08h); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	TempSensClear	reserved			MFCrypto1On	ModemState[2:0]		
Access	R/W	-			D	R		

**Table 31. Status2Reg register bit descriptions**

Bit	Symbol	Value	Description
7	TempSensClear	1	clears the temperature error if the temperature is below the alarm limit of 125 °C
6 to 4	reserved	-	reserved
3	MFCrypto1On	-	indicates that the MIFARE Crypto1 unit is switched on and therefore all data communication with the card is encrypted can only be set to logic 1 by a successful execution of the MFAuthent command only valid in Read/Write mode for MIFARE standard cards this bit is cleared by software
2 to 0	ModemState[2:0]	-	shows the state of the transmitter and receiver state machines:
		000	idle
		001	wait for the BitFramingReg register's StartSend bit
		010	TxWait: wait until RF field is present if the TModeReg register's TxWaitRF bit is set to logic 1 the minimum time for TxWait is defined by the TxWaitReg register
		011	transmitting
		100	RxWait: wait until RF field is present if the TModeReg register's TxWaitRF bit is set to logic 1 the minimum time for RxWait is defined by the RxWaitReg register
		101	wait for data
		110	receiving

### 9.3.1.10 FIFODataReg register

Input and output of 64 byte FIFO buffer.

**Table 32. FIFODataReg register (address 09h); reset value: xxh bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	FIFOData[7:0]							
Access	D							

**Table 33. FIFODataReg register bit descriptions**

Bit	Symbol	Description
7 to 0	FIFOData[7:0]	data input and output port for the internal 64-byte FIFO buffer FIFO buffer acts as parallel in/parallel out converter for all serial data stream inputs and outputs

### 9.3.1.11 FIFOLevelReg register

Indicates the number of bytes stored in the FIFO.

**Table 34. FIFOLevelReg register (address 0Ah); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0	
Symbol	FlushBuffer	FIFOLevel[6:0]							
Access	W	R							

**Table 35. FIFOLevelReg register bit descriptions**

Bit	Symbol	Value	Description
7	FlushBuffer	1	immediately clears the internal FIFO buffer's read and write pointer and ErrorReg register's BufferOvfl bit reading this bit always returns 0
6 to 0	FIFOLevel [6:0]	-	indicates the number of bytes stored in the FIFO buffer writing to the FIFODataReg register increments and reading decrements the FIFOLevel value

### 9.3.1.12 WaterLevelReg register

Defines the level for FIFO under- and overflow warning.

**Table 36. WaterLevelReg register (address 0Bh); reset value: 08h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			WaterLevel[5:0]				
Access	-			R/W				

**Table 37. WaterLevelReg register bit descriptions**

Bit	Symbol	Description
7 to 6	reserved	reserved for future use
5 to 0	WaterLevel [5:0]	<p>defines a warning level to indicate a FIFO buffer overflow or underflow:</p> <p>Status1Reg register's HiAlert bit is set to logic 1 if the remaining number of bytes in the FIFO buffer space is equal to, or less than the defined number of WaterLevel bytes</p> <p>Status1Reg register's LoAlert bit is set to logic 1 if equal to, or less than the WaterLevel bytes in the FIFO buffer</p> <p><b>Remark:</b> to calculate values for HiAlert and LoAlert see <a href="#">Section 9.3.1.8 on page 26</a>.</p>

### 9.3.1.13 ControlReg register

Miscellaneous control bits.

**Table 38. ControlReg register (address 0Ch); reset value: 10h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	TStopNow	TStartNow		reserved			RxLastBits[2:0]	
Access	W	W		-			R	

**Table 39. ControlReg register bit descriptions**

Bit	Symbol	Value	Description
7	TStopNow	1	timer stops immediately reading this bit always returns it to logic 0
6	TStartNow	1	timer starts immediately reading this bit always returns it to logic 0
5 to 3	reserved	-	reserved for future use
2 to 0	RxLastBits[2:0]	-	indicates the number of valid bits in the last received byte if this value is 000b, the whole byte is valid

### 9.3.1.14 BitFramingReg register

Adjustments for bit-oriented frames.

**Table 40. BitFramingReg register (address 0Dh); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	StartSend	RxAlign[2:0]			reserved	TxLastBits[2:0]		
Access	W	R/W			-	R/W		

**Table 41. BitFramingReg register bit descriptions**

Bit	Symbol	Value	Description
7	StartSend	1	starts the transmission of data only valid in combination with the Transceive command
6 to 4	RxAlign[2:0]		used for reception of bit-oriented frames: defines the bit position for the first bit received to be stored in the FIFO buffer example:
		0	LSB of the received bit is stored at bit position 0, the second received bit is stored at bit position 1
		1	LSB of the received bit is stored at bit position 1, the second received bit is stored at bit position 2
		7	LSB of the received bit is stored at bit position 7, the second received bit is stored in the next byte that follows at bit position 0  These bits are only to be used for bitwise anticollision at 106 kBd, for all other modes they are set to 0
3	reserved	-	reserved for future use
2 to 0	TxLastBits[2:0]	-	used for transmission of bit oriented frames: defines the number of bits of the last byte that will be transmitted 000b indicates that all bits of the last byte will be transmitted

### 9.3.1.15 CollReg register

Defines the first bit-collision detected on the RF interface.

**Table 42. CollReg register (address 0Eh); reset value: xxh bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	ValuesAfterColl	reserved	CollPosNotValid	CollPos[4:0]				
Access	R/W	-	R	R				

**Table 43. CollReg register bit descriptions**

Bit	Symbol	Value	Description
7	ValuesAfterColl	0	all received bits will be cleared after a collision only used during bitwise anticollision at 106 kBd, otherwise it is set to logic 1
6	reserved	-	reserved for future use
5	CollPosNotValid	1	no collision detected or the position of the collision is out of the range of CollPos[4:0]

**Table 43. CollReg register bit descriptions ...continued**

Bit	Symbol	Value	Description
4 to 0	CollPos[4:0]	-	shows the bit position of the first detected collision in a received frame only data bits are interpreted example:
		00h	indicates a bit-collision in the 32 <sup>nd</sup> bit
		01h	indicates a bit-collision in the 1 <sup>st</sup> bit
		08h	indicates a bit-collision in the 8 <sup>th</sup> bit
			These bits will only be interpreted if the CollPosNotValid bit is set to logic 0

### 9.3.1.16 Reserved register 0Fh

Functionality is reserved for future use.

**Table 44. Reserved register (address 0Fh); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol								reserved
Access								-

**Table 45. Reserved register bit descriptions**

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

## 9.3.2 Page 1: Communication

### 9.3.2.1 Reserved register 10h

Functionality is reserved for future use.

**Table 46. Reserved register (address 10h); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol								reserved
Access								-

**Table 47. Reserved register bit descriptions**

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

### 9.3.2.2 ModeReg register

Defines general mode settings for transmitting and receiving.

**Table 48. ModeReg register (address 11h); reset value: 3Fh bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	MSBFirst	reserved	TxWaitRF	reserved	PolMFin	reserved	CRCPreset[1:0]	
Access	R/W	-	R/W	-	R/W	-	R/W	

**Table 49. ModeReg register bit descriptions**

Bit	Symbol	Value	Description
7	MSBFirst	1	CRC coprocessor calculates the CRC with MSB first in the CRCResultReg register the values for the CRCResultMSB[7:0] bits and the CRCResultLSB[7:0] bits are bit reversed <b>Remark:</b> during RF communication this bit is ignored
6	reserved	-	reserved for future use
5	TxWaitRF	1	transmitter can only be started if an RF field is generated
4	reserved	-	reserved for future use
3	PolMFin		defines the polarity of pin MFIN <b>Remark:</b> the internal envelope signal is encoded active LOW, changing this bit generates a MFinActIRq event
		1	polarity of pin MFIN is active HIGH
		0	polarity of pin MFIN is active LOW
2	reserved	-	reserved for future use
1 to 0	CRCPreset [1:0]		defines the preset value for the CRC coprocessor for the CalcCRC command <b>Remark:</b> during any communication, the preset values are selected automatically according to the definition of bits in the RxModeReg and TxModeReg registers
		00	0000h
		01	6363h
		10	A671h
		11	FFFFh

### 9.3.2.3 TxModeReg register

Defines the data rate during transmission.

**Table 50. TxModeReg register (address 12h); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	TxCRCEn	TxSpeed[2:0]			InvMod	reserved		
Access	R/W	D			R/W	-		

Table 51. TxModeReg register bit descriptions

Bit	Symbol	Value	Description
7	TxCRCEn	1	enables CRC generation during data transmission <b>Remark:</b> can only be set to logic 0 at 106 kBd
6 to 4	TxSpeed[2:0]		defines the bit rate during data transmission the MF CV520 handles transfer speeds up to 848 kBd
		000	106 kBd
		001	212 kBd
		010	424 kBd
		011	848 kBd
		100	reserved
		101	reserved
		110	reserved
		111	reserved
3	InvMod	1	modulation of transmitted data is inverted
2 to 0	reserved	-	reserved for future use

#### 9.3.2.4 RxModeReg register

Defines the data rate during reception.

Table 52. RxModeReg register (address 13h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RxCRCEn	RxSpeed[2:0]			RxNoErr	RxMultiple	reserved	
Access	R/W	D			R/W	R/W	-	

Table 53. RxModeReg register bit descriptions

Bit	Symbol	Value	Description
7	RxCRCEn	1	enables the CRC calculation during reception <b>Remark:</b> can only be set to logic 0 at 106 kBd
6 to 4	RxSpeed[2:0]		defines the bit rate while receiving data the MF CV520 handles transfer speeds up to 848 kBd
		000	106 kBd
		001	212 kBd
		010	424 kBd
		011	848 kBd
		100	reserved
		101	reserved
		110	reserved
		111	reserved
3	RxNoErr	1	an invalid received data stream (less than 4 bits received) will be ignored and the receiver remains active

**Table 53. RxModeReg register bit descriptions ...continued**

Bit	Symbol	Value	Description
2	RxMultiple	0	receiver is deactivated after receiving a data frame
		1	able to receive more than one data frame only valid for data rates above 106 kBd in order to handle the polling command after setting this bit the Receive and Transceive commands will not terminate automatically. Multiple reception can only be deactivated by writing any command (except the Receive command) to the CommandReg register, or by the host clearing the bit if set to logic 1, an error byte is added to the FIFO buffer at the end of a received data stream which is a copy of the ErrorReg register value
1 to 0	reserved	-	reserved for future use

### 9.3.2.5 TxControlReg register

Controls the logical behavior of the antenna driver pins TX1 and TX2.

**Table 54. TxControlReg register (address 14h); reset value: 80h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	InvTx2RFOn	InvTx1RFOn	InvTx2RFOff	InvTx1RFOff	Tx2CW	reserved	Tx2RFEn	Tx1RFEn
Access	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W

**Table 55. TxControlReg register bit descriptions**

Bit	Symbol	Value	Description
7	InvTx2RFOn	1	output signal on pin TX2 inverted when driver TX2 is enabled
6	InvTx1RFOn	1	output signal on pin TX1 inverted when driver TX1 is enabled
5	InvTx2RFOff	1	output signal on pin TX2 inverted when driver TX2 is disabled
4	InvTx1RFOff	1	output signal on pin TX1 inverted when driver TX1 is disabled
3	Tx2CW	1	output signal on pin TX2 continuously delivers the unmodulated 13.56 MHz energy carrier
		0	Tx2CW bit is enabled to modulate the 13.56 MHz energy carrier
2	reserved	-	reserved for future use
1	Tx2RFEn	1	output signal on pin TX2 delivers the 13.56 MHz energy carrier modulated by the transmission data
0	Tx1RFEn	1	output signal on pin TX1 delivers the 13.56 MHz energy carrier modulated by the transmission data

### 9.3.2.6 TxASKReg register

Controls transmit modulation settings.

**Table 56. TxASKReg register (address 15h); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	Force100ASK	reserved					
Access	-	R/W	-					

**Table 57. TxASKReg register bit descriptions**

Bit	Symbol	Value	Description
7	reserved	-	reserved for future use
6	Force100ASK	1	forces a 100 % ASK modulation independent of the ModGsPReg register setting
5 to 0	reserved	-	reserved for future use

### 9.3.2.7 TxSelReg register

Selects the internal sources for the analog module.

**Table 58. TxSelReg register (address 16h); reset value: 10h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol:	reserved		DriverSel[1:0]		MFOutSel[3:0]			
Access:	-		R/W		R/W			

**Table 59. TxSelReg register bit descriptions**

Bit	Symbol	Value	Description
7 to 6	reserved	-	reserved for future use
5 to 4	DriverSel [1:0]	-	selects the input of drivers TX1 and TX2
		00	3-state; in soft power-down the drivers are only in 3-state mode if the DriverSel[1:0] value is set to 3-state mode
		01	modulation signal (envelope) from the internal encoder, Miller pulse encoded
		10	modulation signal (envelope) from pin MFIN
		11	HIGH; the HIGH level depends on the setting of bits InvTx1RFOn/InvTx1RFOff and InvTx2RFOn/InvTx2RFOff

**Table 59. TxSelReg register bit descriptions ...continued**

Bit	Symbol	Value	Description
3 to 0	MFOutSel [3:0]		selects the input for pin MFOUT
		0000	3-state
		0001	LOW
		0010	HIGH
		0011	test bus signal as defined by the TestSel1Reg register's TstBusBitSel[2:0] value
		0100	modulation signal (envelope) from the internal encoder, Miller pulse encoded
		0101	serial data stream to be transmitted, data stream before Miller encoder
		0110	reserved
		0111	serial data stream received, data stream after Manchester decoder
		1000 to 1111	

### 9.3.2.8 RxSelReg register

Selects internal receiver settings.

**Table 60. RxSelReg register (address 17h); reset value: 84h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	UARTSel[1:0]				RxWait[5:0]			
Access	R/W				R/W			

**Table 61. RxSelReg register bit descriptions**

Bit	Symbol	Value	Description
7 to 6	UARTSel [1:0]		selects the input of the contactless UART
		00	constant LOW
		01	Manchester with subcarrier from pin MFIN
		10	modulated signal from the internal analog module, default
		11	NRZ coding without subcarrier from pin MFIN which is only valid for transfer speeds above 106 kBd
5 to 0	RxWait [5:0]	-	<p>after data transmission the activation of the receiver is delayed for RxWait bit-clocks, during this 'frame guard time' any signal on pin RX is ignored</p> <p>this parameter is ignored by the Receive command</p> <p>all other commands, such as Transceive, MFAuthent use this parameter</p> <p>the counter starts immediately after the external RF field is switched on</p>

### 9.3.2.9 RxThresholdReg register

Selects thresholds for the bit decoder.

**Table 62. RxThresholdReg register (address 18h); reset value: 84h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	MinLevel[3:0]			reserved		CollLevel[2:0]		
Access	R/W			-		R/W		

**Table 63. RxThresholdReg register bit descriptions**

Bit	Symbol	Description
7 to 4	MinLevel [3:0]	defines the minimum signal strength at the decoder input that will be accepted if the signal strength is below this level it is not evaluated
3	reserved	reserved for future use
2 to 0	CollLevel [2:0]	defines the minimum signal strength at the decoder input that must be reached by the weaker half-bit of the Manchester encoded signal to generate a bit-collision relative to the amplitude of the stronger half-bit

### 9.3.2.10 DemodReg register

Defines demodulator settings.

**Table 64. DemodReg register (address 19h); reset value: 4Dh bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	AddIQ[1:0]		FixIQ	TPrescal Even	TauRcv[1:0]		TauSync[1:0]	
Access	R/W		R/W	R/W	R/W		R/W	

**Table 65. DemodReg register bit descriptions**

Bit	Symbol	Value	Description
7 to 6	AddIQ [1:0]	-	defines the use of I and Q channel during reception <b>Remark:</b> the FixIQ bit must be set to logic 0 to enable the following settings:
		00	selects the stronger channel
		01	selects the stronger channel and freezes the selected channel during communication
		10	reserved
		11	reserved
5	FixIQ	1	if AddIQ[1:0] are set to X0b, the reception is fixed to I channel if AddIQ[1:0] are set to X1b, the reception is fixed to Q channel

**Table 65. DemodReg register bit descriptions ...continued**

Bit	Symbol	Value	Description
4	TPrescalEven	R/W	If set to logic 0 the following formula is used to calculate the timer frequency of the prescaler: $f_{\text{timer}} = 13.56 \text{ MHz} / (2 \cdot \text{TPreScaler} + 1).$ If set to logic 1 the following formula is used to calculate the timer frequency of the prescaler: $f_{\text{timer}} = 13.56 \text{ MHz} / (2 \cdot \text{TPreScaler} + 2).$ (Default TPrescalEven bit is logic 0)
3 to 2	TauRcv[1:0]	-	changes the time-constant of the internal PLL during data reception <b>Remark:</b> if set to 00b the PLL is frozen during data reception
1 to 0	TauSync[1:0]	-	changes the time-constant of the internal PLL during burst

**9.3.2.11 Reserved register 1Ah**

Functionality is reserved for future use.

**Table 66. Reserved register (address 1Ah); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol				reserved				
Access				-				

**Table 67. Reserved register bit descriptions**

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

**9.3.2.12 Reserved register 1Bh**

Functionality is reserved for future use.

**Table 68. Reserved register (address 1Bh); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol				reserved				
Access				-				

**Table 69. Reserved register bit descriptions**

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

**9.3.2.13 MfTxReg register**

Controls some MIFARE communication transmit parameters.

**Table 70. MfTxReg register (address 1Ch); reset value: 62h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol				reserved			TxWait[1:0]	
Access				-			R/W	

**Table 71. MfTxReg register bit descriptions**

Bit	Symbol	Description
7 to 2	reserved	reserved for future use
1 to 0	TxWait	defines the additional response time 7 bits are added to the value of the register bit by default

**9.3.2.14 MfRxReg register****Table 72. MfRxReg register (address 1Dh); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			ParityDisable	reserved			
Access	-			R/W	-			

**Table 73. MfRxReg register bit descriptions**

Bit	Symbol	Value	Description
7 to 5	reserved	-	reserved for future use
4	ParityDisable	1	generation of the parity bit for transmission and the parity check for receiving is switched off the received parity bit is handled like a data bit
3 to 0	reserved	-	reserved for future use

**9.3.2.15 Reserved register 1Eh**

Functionality is reserved for future use.

**Table 74. Reserved register (address 1Eh); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

**Table 75. Reserved register bit descriptions**

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

**9.3.2.16 Reserved register 1Fh**

Functionality is reserved for future use.

### 9.3.3 Page 2: Configuration

#### 9.3.3.1 Reserved register 20h

Functionality is reserved for future use.

**Table 76. Reserved register (address 20h); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	-							
Access	reserved							

**Table 77. Reserved register bit descriptions**

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

#### 9.3.3.2 CRCResultReg registers

Shows the MSB and LSB values of the CRC calculation.

**Remark:** The CRC is split into two 8-bit registers.

**Table 78. CRCResultReg (higher bits) register (address 21h); reset value: FFh bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	CRCResultMSB[7:0]							
Access	R							

**Table 79. CRCResultReg register higher bit descriptions**

Bit	Symbol	Description
7 to 0	CRCResultMSB [7:0]	shows the value of the CRCResultReg register's most significant byte only valid if Status1Reg register's CRCReady bit is set to logic 1

**Table 80. CRCResultReg (lower bits) register (address 22h); reset value: FFh bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	CRCResultLSB[7:0]							
Access	R							

**Table 81. CRCResultReg register lower bit descriptions**

Bit	Symbol	Description
7 to 0	CRCResultLSB [7:0]	shows the value of the least significant byte of the CRCResultReg register only valid if Status1Reg register's CRCReady bit is set to logic 1

### 9.3.3.3 Reserved register 23h

Functionality is reserved for future use.

**Table 82. Reserved register (address 23h); reset value: 88h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

**Table 83. Reserved register bit descriptions**

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

### 9.3.3.4 ModWidthReg register

Sets the modulation width.

**Table 84. ModWidthReg register (address 24h); reset value: 26h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	ModWidth[7:0]							
Access	R/W							

**Table 85. ModWidthReg register bit descriptions**

Bit	Symbol	Description
7 to 0	ModWidth[7:0]	defines the width of the Miller modulation as multiples of the carrier frequency ( $\text{ModWidth} + 1 / f_{\text{clk}}$ ) the maximum value is half the bit period

### 9.3.3.5 Reserved register 25h

Functionality is reserved for future use.

**Table 86. Reserved register (address 25h); reset value: 87h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

**Table 87. Reserved register bit descriptions**

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

### 9.3.3.6 RFCfgReg register

Configures the receiver gain.

**Table 88. RFCfgReg register (address 26h); reset value: 48h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	RxGain[2:0]			reserved			
Access	-	R/W			-			

**Table 89. RFCfgReg register bit descriptions**

Bit	Symbol	Value	Description
7	reserved	-	reserved for future use
6 to 4	RxGain [2:0]		defines the receiver's signal voltage gain factor:
		000	18 dB
		001	23 dB
		010	18 dB
		011	23 dB
		100	33 dB
		101	38 dB
		110	43 dB
		111	48 dB
3 to 0	reserved	-	reserved for future use

### 9.3.3.7 GsNReg register

Defines the conductance of the antenna driver pins TX1 and TX2 for the n-driver when the driver is switched on.

**Table 90. GsNReg register (address 27h); reset value: 88h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	CWGsN[3:0]			ModGsN[3:0]				
Access	R/W			R/W				

**Table 91. GsNReg register bit descriptions**

Bit	Symbol	Description
7 to 4	CWGsn [3:0]	<p>defines the conductance of the output n-driver during periods without modulation which can be used to regulate the output power and subsequently current consumption and operating distance</p> <p><b>Remark:</b> the conductance value is binary-weighted during soft Power-down mode the highest bit is forced to logic 1 value is only used if driver TX1 or TX2 is switched on</p>
3 to 0	ModGsN [3:0]	<p>defines the conductance of the output n-driver during periods without modulation which can be used to regulate the modulation index</p> <p><b>Remark:</b> the conductance value is binary weighted during soft Power-down mode the highest bit is forced to logic 1 value is only used if driver TX1 or TX2 is switched on</p>

### 9.3.3.8 CWGsPReg register

Defines the conductance of the p-driver output during periods of no modulation.

**Table 92. CWGsPReg register (address 28h); reset value: 20h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		CWGsP[5:0]					
Access	-		R/W					

**Table 93. CWGsPReg register bit descriptions**

Bit	Symbol	Description
7 to 6	reserved	reserved for future use
5 to 0	CWGSP[5:0]	defines the conductance of the p-driver output which can be used to regulate the output power and subsequently current consumption and operating distance <b>Remark:</b> the conductance value is binary weighted during soft Power-down mode the highest bit is forced to logic 1

### 9.3.3.9 ModGsPReg register

Defines the conductance of the p-driver output during modulation.

**Table 94. ModGsPReg register (address 29h); reset value: 20h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		ModGsP[5:0]					
Access	-		R/W					

**Table 95. ModGsPReg register bit descriptions**

Bit	Symbol	Description
7 to 6	reserved	reserved for future use
5 to 0	ModGsP[5:0]	defines the conductance of the p-driver output during modulation which can be used to regulate the modulation index <b>Remark:</b> the conductance value is binary weighted during soft Power-down mode the highest bit is forced to logic 1 if the TxASKReg register's Force100ASK bit is set to logic 1 the value of ModGsP has no effect

### 9.3.3.10 TModeReg and TPrescalerReg registers

These registers define the timer settings.

**Remark:** The TPrescaler setting higher 4 bits are in the TModeReg register and the lower 8 bits are in the TPrescalerReg register.

**Table 96. TModeReg register (address 2Ah); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	TAuto	TGated[1:0]		TAutoRestart	TPrescaler_Hi[3:0]			
Access	R/W	R/W		R/W	R/W			

**Table 97. TModeReg register bit descriptions**

Bit	Symbol	Value	Description
7	TAuto	1	timer starts automatically at the end of the transmission in all communication modes at all speeds if the RxModeReg register's RxMultiple bit is not set, the timer stops immediately after receiving the 5th bit (1 start bit, 4 data bits) if the RxMultiple bit is set to logic 1 the timer never stops, in which case the timer can be stopped by setting the ControlReg register's TStopNow bit to logic 1
		0	indicates that the timer is not influenced by the protocol
6 to 5	TGated[1:0]		internal timer is running in gated mode <b>Remark:</b> in gated mode, the Status1Reg register's TRunning bit is logic 1 when the timer is enabled by the TModeReg register's TGated[1:0] bits this bit does not influence the gating signal
		00	non-gated mode
		01	gated by pin MFIN
		10	gated by pin AUX1
		11	-
4	TAutoRestart	1	timer automatically restarts its count-down from the 16-bit timer reload value instead of counting down to zero
		0	timer decrements to 0 and the ComlRqReg register's TimerIRq bit is set to logic 1
3 to 0	TPrescaler_Hi[3:0]	-	defines the higher 4 bits of the TPrescaler value The following formula is used to calculate the timer frequency if the DemodReg register's TPrescalEven bit in Demot Regis set to logic 0: $f_{\text{timer}} = 13.56 \text{ MHz} / (2^*TPreScaler+1).$ Where TPreScaler = [TPrescaler_Hi:TPrescaler_Lo] (TPrescaler value on 12 bits) (Default TPrescalEven bit is logic 0) The following formula is used to calculate the timer frequency if the DemodReg register's TPrescalEven bit is set to logic 1: $f_{\text{timer}} = 13.56 \text{ MHz} / (2^*TPreScaler+2).$ See <a href="#">Section 8.5 "Timer unit"</a> .

**Table 98. TPrescalerReg register (address 2Bh); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	TPrescaler_Lo[7:0]							
Access	R/W							

**Table 99. TPrescalerReg register bit descriptions**

Bit	Symbol	Description
7 to 0	TPrescaler_Lo[7:0]	<p>defines the lower 8 bits of the TPrescaler value</p> <p>The following formula is used to calculate the timer frequency if the DemodReg register's TPrescalEven bit is set to logic 0:</p> $f_{\text{timer}} = 13.56 \text{ MHz} / (2 * \text{TPreScaler} + 1).$ <p>Where TPreScaler = [TPrescaler_Hi:TPrescaler_Lo] (TPrescaler value on 12 bits) (Default TPrescalEven bit is logic 0)</p> <p>The following formula is used to calculate the timer frequency if the DemodReg register's TPrescalEven bit in DemoReg is set to logic 1:</p> $f_{\text{timer}} = 13.56 \text{ MHz} / (2 * \text{TPreScaler} + 2).$ <p>See <a href="#">Section 8.5 "Timer unit"</a>.</p>

### 9.3.3.11 TReloadReg register

Defines the 16-bit timer reload value.

**Remark:** The reload value bits are contained in two 8-bit registers.

**Table 100. TReloadReg (higher bits) register (address 2Ch); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	TReloadVal_Hi[7:0]							
Access	R/W							

**Table 101. TReloadReg register higher bit descriptions**

Bit	Symbol	Description
7 to 0	TReloadVal_Hi[7:0]	<p>defines the higher 8 bits of the 16-bit timer reload value</p> <p>on a start event, the timer loads the timer reload value</p> <p>changing this register affects the timer only at the next start event</p>

**Table 102. TReloadReg (lower bits) register (address 2Dh); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	TReloadVal_Lo[7:0]							
Access	R/W							

**Table 103. TReloadReg register lower bit descriptions**

Bit	Symbol	Description
7 to 0	TReloadVal_Lo[7:0]	<p>defines the lower 8 bits of the 16-bit timer reload value</p> <p>on a start event, the timer loads the timer reload value</p> <p>changing this register affects the timer only at the next start event</p>

### 9.3.3.12 TCounterValReg register

Contains the timer value.

**Remark:** The timer value bits are contained in two 8-bit registers.

**Table 104. TCounterValReg (higher bits) register (address 2Eh); reset value: xxh bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	TCounterVal_Hi[7:0]							
Access	R							

**Table 105. TCounterValReg register higher bit descriptions**

Bit	Symbol	Description
7 to 0	TCounterVal_Hi [7:0]	timer value higher 8 bits

**Table 106. TCounterValReg (lower bits) register (address 2Fh); reset value: xxh bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	TCounterVal_Lo[7:0]							
Access	R							

**Table 107. TCounterValReg register lower bit descriptions**

Bit	Symbol	Description
7 to 0	TCounterVal_Lo [7:0]	timer value lower 8 bits

### 9.3.4 Page 3: Test

#### 9.3.4.1 Reserved register 30h

Functionality is reserved for future use.

**Table 108. Reserved register (address 30h); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

**Table 109. Reserved register bit descriptions**

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

#### 9.3.4.2 TestSel1Reg register

General test signal configuration.

**Table 110. TestSel1Reg register (address 31h); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	reserved					TstBusBitSel[2:0]		
Access	-					R/W		

**Table 111. TestSel1Reg register bit descriptions**

Bit	Symbol	Description
7 to 3	reserved	reserved for future use
2 to 0	TstBusBitSel [2:0]	selects a test bus signal which is output at pin MFOUT if AnalogSelAux2[3:0] = FFh in AnalogTestReg register, test bus signal is also output at pins AUX1 or AUX2

### 9.3.4.3 TestSel2Reg register

General test signal configuration and PRBS control.

**Table 112. TestSel2Reg register (address 32h); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	TstBusFlip	PRBS9	PRBS15	TestBusSel[4:0]				
Access	R/W	R/W	R/W	R/W				

**Table 113. TestSel2Reg register bit descriptions**

Bit	Symbol	Value	Description
7	TstBusFlip	1	test bus is mapped to the parallel port in the following order: TstBusBit4, TstBusBit3, TstBusBit2, TstBusBit6, TstBusBit5, TstBusBit0; see <a href="#">Section 16.1 on page 63</a>
6	PRBS9	-	starts and enables the PRBS9 sequence according to ITU-TO150 <b>Remark:</b> all relevant registers to transmit data must be configured before entering PRBS9 mode the data transmission of the defined sequence is started by the Transmit command
5	PRBS15	-	starts and enables the PRBS15 sequence according to ITU-TO150 <b>Remark:</b> all relevant registers to transmit data must be configured before entering PRBS15 mode the data transmission of the defined sequence is started by the Transmit command
4 to 0	TestBusSel[4:0]	-	selects the test bus; see <a href="#">Section 16.1 "Test signals"</a>

### 9.3.4.4 TestPinEnReg register

Enables the test bus pin output driver.

**Table 114. TestPinEnReg register (address 33h); reset value: 80h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	TestPinEn[5:0]					reserved	
Access	-	R/W					-	

**Table 115. TestPinEnReg register bit descriptions**

Bit	Symbol	Value	Description
7	reserved	-	reserved for future use
6 to 1	TestPinEn [5:0]	-	enables the output driver on one of the data pins D1 to D7 which outputs a test signal <b>Example:</b> setting bit 1 to logic 1 enables pin D1 output setting bit 5 to logic 1 enables pin D5 output <b>Remark:</b> If the SPI is used, only pins D1 to D4 can be used. If the serial UART interface is used and the RS232LineEn bit is set to logic 1 only pins D1 to D4 can be used.
0	reserved	-	reserved for future use

#### 9.3.4.5 TestPinValueReg register

Defines the HIGH and LOW values for the test port D1 to D7 when it is used as I/O.

**Table 116. TestPinValueReg register (address 34h); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	UseIO		TestPinValue[5:0]					reserved
Access	R/W		R/W					-

**Table 117. TestPinValueReg register bit descriptions**

Bit	Symbol	Value	Description
7	UseIO	1	enables the I/O functionality for the test port when one of the serial interfaces is used the input/output behavior is defined by value TestPinEn[5:0] in the TestPinEnReg register the value for the output behavior is defined by TestPinValue[5:0]
6 to 1	TestPinValue [5:0]	-	defines the value of the test port when it is used as I/O and each output must be enabled by TestPinEn[5:0] in the TestPinEnReg register <b>Remark:</b> Reading the register indicates the status of pins D6 to D1 if the UseIO bit is set to logic 1. If the UseIO bit is set to logic 0, the value of the TestPinValueReg register is read back.
0	reserved	-	reserved for future use

#### 9.3.4.6 TestBusReg register

Shows the status of the internal test bus.

**Table 118. TestBusReg register (address 35h); reset value: xxh bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	TestBus[7:0]							
Access	R							

**Table 119. TestBusReg register bit descriptions**

Bit	Symbol	Description
7 to 0	TestBus[7:0]	shows the status of the internal test bus the test bus is selected using the TestSel2Reg register; see <a href="#">Section 16.1 on page 63</a>

**9.3.4.7 AutoTestReg register**

Controls the digital self-test.

**Table 120. AutoTestReg register (address 36h); reset value: 40h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	AmpRcv	RFT		SelfTest[3:0]			
Access	-	R/W	-		R/W			

**Table 121. AutoTestReg register bit descriptions**

Bit	Symbol	Value	Description
7	reserved	-	reserved for production tests
6	AmpRcv	1	internal signal processing in the receiver chain is performed non-linearly which increases the operating distance in communication modes at 106 kBd <b>Remark:</b> due to non-linearity, the effect of the RxThresholdReg register's MinLevel[3:0] and the CollLevel[2:0] values is also non-linear
5 to 4	RFT	-	reserved for production tests
3 to 0	SelfTest[3:0]	-	enables the digital self test the self test can also be started by the CalcCRC command; see <a href="#">Section 10.3.1.3 on page 54</a> the self test is enabled by value 1001b <b>Remark:</b> for default operation the self test must be disabled by value 0000b

**9.3.4.8 VersionReg register**

Shows the MF CV520 software version.

**Table 122. VersionReg register (address 37h); reset value: xxh bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	Version[7:0]							
Access	R							

**Table 123. VersionReg register bit descriptions**

Bit	Symbol	Description
7 to 0	Version[7:0]	indicates current software version of the MF CV520 <b>Remark:</b> the current version of the MF CV520 is 92h

**9.3.4.9 AnalogTestReg register**

Determines the analog output test signal at, and status of, pins AUX1 and AUX2.

**Table 124. AnalogTestReg register (address 38h); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	AnalogSelAux1[3:0]				AnalogSelAux2[3:0]			
Access	R/W				R/W			

**Table 125. AnalogTestReg register bit descriptions**

Bit	Symbol	Value	Description
7 to 4	AnalogSelAux1 [3:0]		controls pin AUX1
		0000	3-state
		0001	output of TestDAC1 (AUX1), output of TestDAC2 (AUX2) <sup>[1]</sup>
		0010	test signal Corr1 <sup>[1]</sup>
		0011	reserved
		0100	DAC: test signal MinLevel <sup>[1]</sup>
		0101	DAC: test signal ADC_I <sup>[1]</sup>
		0110	DAC: test signal ADC_Q <sup>[1]</sup>
		0111	reserved
		1000	reserved, test signal for production test <sup>[1]</sup>
		1001	reserved
		1010	HIGH
		1011	LOW
		1100	TxActive: at 106 kBd: HIGH during Start bit, Data bit, Parity and CRC at 212 kBd: 424 kBd and 848 kBd: HIGH during data and CRC
		1101	RxActive: at 106 kBd: HIGH during Data bit, Parity and CRC at 212 kBd: 424 kBd and 848 kBd: HIGH during data and CRC
		1110	subcarrier detected: 106 kBd: not applicable 212 kBd: 424 kBd and 848 kBd: HIGH during last part of data and CRC
		1111	test bus bit as defined by the TestSel1Reg register's TstBusBitSel[2:0] bits <b>Remark:</b> all test signals are described in <a href="#">Section 16.1 on page 63</a>
3 to 0	AnalogSelAux2 [3:0]	-	controls pin AUX2 (see bit descriptions for AUX1)

[1] **Remark:** Current source output; the use of 1 kΩ pull-down resistor on AUXn is recommended.

### 9.3.4.10 TestDAC1Reg register

Defines the test value for TestDAC1.

**Table 126. TestDAC1Reg register (address 39h); reset value: xxh bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		TestDAC1[5:0]					
Access	-		R/W					

**Table 127. TestDAC1Reg register bit descriptions**

Bit	Symbol	Description
7	reserved	reserved for production tests
6	reserved	reserved for future use
5 to 0	TestDAC1[5:0]	defines the test value for TestDAC1 output of DAC1 can be routed to AUX1 by setting value AnalogSelAux1[3:0] to 0001b in the AnalogTestReg register

### 9.3.4.11 TestDAC2Reg register

Defines the test value for TestDAC2.

**Table 128. TestDAC2Reg register (address 3Ah); reset value: xxh bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		TestDAC2[5:0]					
Access	-		R/W					

**Table 129. TestDAC2Reg register bit descriptions**

Bit	Symbol	Description
7 to 6	reserved	reserved for future use
5 to 0	TestDAC2[5:0]	defines the test value for TestDAC2 output of DAC2 can be routed to AUX2 by setting value AnalogSelAux2[3:0] to 0001b in the AnalogTestReg register

### 9.3.4.12 TestADCReg register

Shows the values of ADC I and Q channels.

**Table 130. TestADCReg register (address 3Bh); reset value: xxh bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol	ADC_I[3:0]			ADC_Q[3:0]				
Access	R			R				

**Table 131. TestADCReg register bit descriptions**

Bit	Symbol	Description
7 to 4	ADC_I[3:0]	ADC I channel value
3 to 0	ADC_Q[3:0]	ADC Q channel value

### 9.3.4.13 Reserved register 3Ch

Functionality reserved for production test.

**Table 132. Reserved register (address 3Ch); reset value: FFh bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol					RFT			
Access					-			

**Table 133. Reserved register bit descriptions**

Bit	Symbol	Description
7 to 0	reserved	reserved for production tests

**Table 134. Reserved register (address 3Dh); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol					RFT			
Access					-			

**Table 135. Reserved register bit descriptions**

Bit	Symbol	Description
7 to 0	reserved	reserved for production tests

**Table 136. Reserved register (address 3Eh); reset value: 03h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol					RFT			
Access					-			

**Table 137. Reserved register bit descriptions**

Bit	Symbol	Description
7 to 0	reserved	reserved for production tests

**Table 138. Reserved register (address 3Fh); reset value: 00h bit allocation**

Bit	7	6	5	4	3	2	1	0
Symbol					reserved			
Access					-			

**Table 139. Reserved register bit descriptions**

Bit	Symbol	Description
7 to 0	reserved	reserved for production tests

## 10. MF CV520 command set

### 10.1 General description

The MF CV520 operation is determined by a state machine capable of performing a set of commands. A command is executed by writing a command code (see [Table 140](#)) to the CommandReg register.

Arguments and/or data necessary to process a command are exchanged via the FIFO buffer.

### 10.2 General behavior

- Each command that needs a data bit stream (or data byte stream) as an input immediately processes any data in the FIFO buffer. An exception to this rule is the Transceive command. Using this command, transmission is started with the BitFramingReg register's StartSend bit.
- Each command that needs a certain number of arguments, starts processing only when it has received the correct number of arguments from the FIFO buffer.
- The FIFO buffer is not automatically cleared when commands start. This makes it possible to write command arguments and/or the data bytes to the FIFO buffer and then start the command.
- Each command can be interrupted by the host writing a new command code to the CommandReg register, for example, the Idle command.

### 10.3 MF CV520 command overview

**Table 140. Command overview**

Command	Command code	Action
Idle	0000	no action, cancels current command execution
Mem	0001	stores 25 bytes into the internal buffer
CalcCRC	0011	activates the CRC coprocessor or performs a self test
Transmit	0100	transmits data from the FIFO buffer
NoCmdChange	0111	no command change, can be used to modify the CommandReg register bits without affecting the command, for example, the PowerDown bit
Receive	1000	activates the receiver circuits
Transceive	1100	transmits data from FIFO buffer to antenna and automatically activates the receiver after transmission
MFAuthent	1110	performs the MIFARE standard authentication as a reader
SoftReset	1111	resets the MF CV520

## 10.3.1 MF CV520 command descriptions

### 10.3.1.1 Idle

Places the MF CV520 in Idle mode. The Idle command also terminates itself.

### 10.3.1.2 Mem

Transfers 25 bytes from the FIFO buffer to the internal buffer.

To read out the 25 bytes from the internal buffer the Mem command must be started with an empty FIFO buffer. In this case, the 25 bytes are transferred from the internal buffer to the FIFO.

During a hard power-down (using pin NRSTPD), the 25 bytes in the internal buffer remain unchanged and are only lost if the power supply is removed from the MF CV520.

This command automatically terminates when finished and the Idle command becomes active.

### 10.3.1.3 CalcCRC

The FIFO buffer content is transferred to the CRC coprocessor and the CRC calculation is started. The calculation result is stored in the CRCResultReg register. The CRC calculation is not limited to a dedicated number of bytes. The calculation is not stopped when the FIFO buffer is empty during the data stream. The next byte written to the FIFO buffer is added to the calculation.

The CRC preset value is controlled by the ModeReg register's CRCPreset[1:0] bits. The value is loaded in to the CRC coprocessor when the command starts.

This command must be terminated by writing a command to the CommandReg register, such as, the Idle command.

If the AutoTestReg register's SelfTest[3:0] bits are set correctly, the MF CV520 enters Self Test mode. Starting the CalcCRC command initiates a digital self test. The result of the self test is written to the FIFO buffer.

### 10.3.1.4 Transmit

The FIFO buffer content is immediately transmitted after starting this command. Before transmitting the FIFO buffer content, all relevant registers must be set for data transmission.

This command automatically terminates when the FIFO buffer is empty. It can be terminated by another command written to the CommandReg register.

### 10.3.1.5 NoCmdChange

This command does not influence any running command in the CommandReg register. It can be used to manipulate any bit except the CommandReg register Command[3:0] bits, for example, the RcvOff bit or the PowerDown bit.

### 10.3.1.6 Receive

The MF CV520 activates the receiver path and waits for a data stream to be received. The correct settings must be chosen before starting this command.

This command automatically terminates when the data stream ends. This is indicated either by the end of frame pattern or by the length byte depending on the selected frame type and speed.

**Remark:** If the RxModeReg register's RxMultiple bit is set to logic 1, the Receive command will not automatically terminate. It must be terminated by starting another command in the CommandReg register.

#### 10.3.1.7 Transceive

This command continuously repeats the transmission of data from the FIFO buffer and the reception of data from the RF field. The first action is transmit and after transmission the command is changed to receive a data stream.

Each transmit process must be started by setting the BitFramingReg register's StartSend bit to logic 1. This command must be cleared by writing any command to the CommandReg register.

**Remark:** If the RxModeReg register's RxMultiple bit is set to logic 1, the Transceive command never leaves the receive state because this state cannot be cancelled automatically.

#### 10.3.1.8 MFAuthent

This command manages MIFARE authentication to enable a secure communication to any MIFARE Mini, MIFARE 1K and MIFARE 4K card. The following data is written to the FIFO buffer before the command can be activated:

- Authentication command code (60h, 61h)
- Block address
- Sector key byte 0
- Sector key byte 1
- Sector key byte 2
- Sector key byte 3
- Sector key byte 4
- Sector key byte 5
- Card serial number byte 0
- Card serial number byte 1
- Card serial number byte 2
- Card serial number byte 3

In total 12 bytes are written to the FIFO.

**Remark:** When the MFAuthent command is active all access to the FIFO buffer is blocked. However, if there is access to the FIFO buffer, the ErrorReg register's WrErr bit is set.

This command automatically terminates when the MIFARE card is authenticated and the Status2Reg register's MFCrypto1On bit is set to logic 1.

This command does not terminate automatically if the card does not answer, so the timer must be initialized to automatic mode. In this case, in addition to the IdleIRq bit, the TimerIRq bit can be used as the termination criteria. During authentication processing, the RxIRq bit and TxIRq bit are blocked. The Crypto1On bit is only valid after termination of the MFAuthent command, either after processing the protocol or writing Idle to the CommandReg register.

If an error occurs during authentication, the ErrorReg register's ProtocolErr bit is set to logic 1 and the Status2Reg register's Crypto1On bit is set to logic 0.

#### 10.3.1.9 SoftReset

This command performs a reset of the device. The configuration data of the internal buffer remains unchanged. All registers are set to the reset values. This command automatically terminates when finished.

## 11. Limiting values

**Table 141. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DDA</sub>	analog supply voltage		-0.5	+4.0	V
V <sub>DDD</sub>	digital supply voltage		-0.5	+4.0	V
V <sub>DD(PVDD)</sub>	PVDD supply voltage		-0.5	+4.0	V
V <sub>DD(TVDD)</sub>	TVDD supply voltage		-0.5	+4.0	V
V <sub>DD(SVDD)</sub>	SVDD supply voltage		-0.5	+4.0	V
V <sub>i</sub>	input voltage	all input pins except pins MFIN and RX	V <sub>SS(PVSS)</sub> - 0.5	V <sub>DD(PVDD)</sub> + 0.5	V
		pin MFIN	V <sub>SS(PVSS)</sub> - 0.5	V <sub>DD(SVDD)</sub> + 0.5	V
P <sub>tot</sub>	total power dissipation	per package; and V <sub>DDD</sub> in shortcut mode	-	200	mW
T <sub>j</sub>	junction temperature		-	100	°C
V <sub>ESD</sub>	electrostatic discharge voltage	HBM; 1500 Ω, 100 pF; JESD22-A114-B	-	2000	V
		MM; 0.75 μH, 200 pF; JESD22-A114-A	-	200	V

## 12. Recommended operating conditions

**Table 142. Operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>DDA</sub>	analog supply voltage	V <sub>DD(PVDD)</sub> ≤ V <sub>DDA</sub> = V <sub>DDD</sub> = V <sub>DD(TVDD)</sub> ; V <sub>SSA</sub> = V <sub>SSD</sub> = V <sub>SS(PVSS)</sub> = V <sub>SS(TVSS)</sub> = 0 V	[1][2] 2.5	3.3	3.6	V
V <sub>DDD</sub>	digital supply voltage	V <sub>DD(PVDD)</sub> ≤ V <sub>DDA</sub> = V <sub>DDD</sub> = V <sub>DD(TVDD)</sub> ; V <sub>SSA</sub> = V <sub>SSD</sub> = V <sub>SS(PVSS)</sub> = V <sub>SS(TVSS)</sub> = 0 V	[1][2] 2.5	3.3	3.6	V
V <sub>DD(TVDD)</sub>	TVDD supply voltage	V <sub>DD(PVDD)</sub> ≤ V <sub>DDA</sub> = V <sub>DDD</sub> = V <sub>DD(TVDD)</sub> ; V <sub>SSA</sub> = V <sub>SSD</sub> = V <sub>SS(PVSS)</sub> = V <sub>SS(TVSS)</sub> = 0 V	[1][2] 2.5	3.3	3.6	V
V <sub>DD(PVDD)</sub>	PVDD supply voltage	V <sub>DD(PVDD)</sub> ≤ V <sub>DDA</sub> = V <sub>DDD</sub> = V <sub>DD(TVDD)</sub> ; V <sub>SSA</sub> = V <sub>SSD</sub> = V <sub>SS(PVSS)</sub> = V <sub>SS(TVSS)</sub> = 0 V	[3] 1.6	1.8	3.6	V
V <sub>DD(SVDD)</sub>	SVDD supply voltage	V <sub>SSA</sub> = V <sub>SSD</sub> = V <sub>SS(PVSS)</sub> = V <sub>SS(TVSS)</sub> = 0 V	1.6	-	3.6	V
T <sub>amb</sub>	ambient temperature	HVQFN32	-25	-	+85	°C

[1] Supply voltages below 3 V reduce the performance (the achievable operating distance).

[2] V<sub>DDA</sub>, V<sub>DDD</sub> and V<sub>DD(TVDD)</sub> must always be the same voltage.

[3] V<sub>DD(PVDD)</sub> must always be the same or lower voltage than V<sub>DDD</sub>.

## 13. Thermal characteristics

**Table 143. Thermal characteristics**

Symbol	Parameter	Conditions	Package	Typ	Unit
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in still air with exposed pin soldered on a 4 layer JEDEC PCB	HVQFN32	40	K/W

## 14. Characteristics

Table 144. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Input characteristics</b>						
<b>NRSTPD</b>						
$I_{LI}$	input leakage current		-1	-	+1	$\mu\text{A}$
$V_{IH}$	HIGH-level input voltage		$0.7V_{DD(PVDD)}$	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	$0.3V_{DD(PVDD)}$	V
<b>Pin MFIN</b>						
$I_{LI}$	input leakage current		-1	-	+1	$\mu\text{A}$
$V_{IH}$	HIGH-level input voltage		$0.7V_{DD(SVDD)}$	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	$0.3V_{DD(SVDD)}$	V
<b>Pin SDA</b>						
$I_{LI}$	input leakage current		-1	-	+1	$\mu\text{A}$
$V_{IH}$	HIGH-level input voltage		$0.7V_{DD(PVDD)}$	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	$0.3V_{DD(PVDD)}$	V
<b>Pin RX<sup>[1]</sup></b>						
$V_i$	input voltage		-1	-	$V_{DDA} + 1$	V
$C_i$	input capacitance	$V_{DDA} = 3\text{ V}$ ; receiver active; $V_{RX(p-p)} = 1\text{ V}$ ; 1.5 V (DC) offset	-	10	-	pF
$R_i$	input resistance	$V_{DDA} = 3\text{ V}$ ; receiver active; $V_{RX(p-p)} = 1\text{ V}$ ; 1.5 V (DC) offset	-	350	-	$\Omega$
<b>Input voltage range; see Figure 12</b>						
$V_{i(p-p)(min)}$	minimum peak-to-peak input voltage	Manchester encoded; $V_{DDA} = 3\text{ V}$	-	100	-	mV
$V_{i(p-p)(max)}$	maximum peak-to-peak input voltage	Manchester encoded; $V_{DDA} = 3\text{ V}$	-	4	-	V
<b>Input sensitivity; see Figure 12</b>						
$V_{mod}$	modulation voltage	minimum Manchester encoded; $V_{DDA} = 3\text{ V}$ ; $RxGain[2:0] = 111\text{b}$ (48 dB)	-	5	-	mV
<b>Pin OSCIN</b>						
$I_{LI}$	input leakage current		-1	-	+1	$\mu\text{A}$
$V_{IH}$	HIGH-level input voltage		$0.7V_{DDA}$	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	$0.3V_{DDA}$	V
$C_i$	input capacitance	$V_{DDA} = 2.8\text{ V}$ ; DC = 0.65 V; AC = 1 V (p-p)	-	2	-	pF
<b>Input/output characteristics</b>						
<b>pins D1, D2, D3, D4, D5, D6 and D7</b>						
$I_{LI}$	input leakage current		-1	-	+1	$\mu\text{A}$
$V_{IH}$	HIGH-level input voltage		$0.7V_{DD(PVDD)}$	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	$0.3V_{DD(PVDD)}$	V

Table 144. Characteristics ...continued

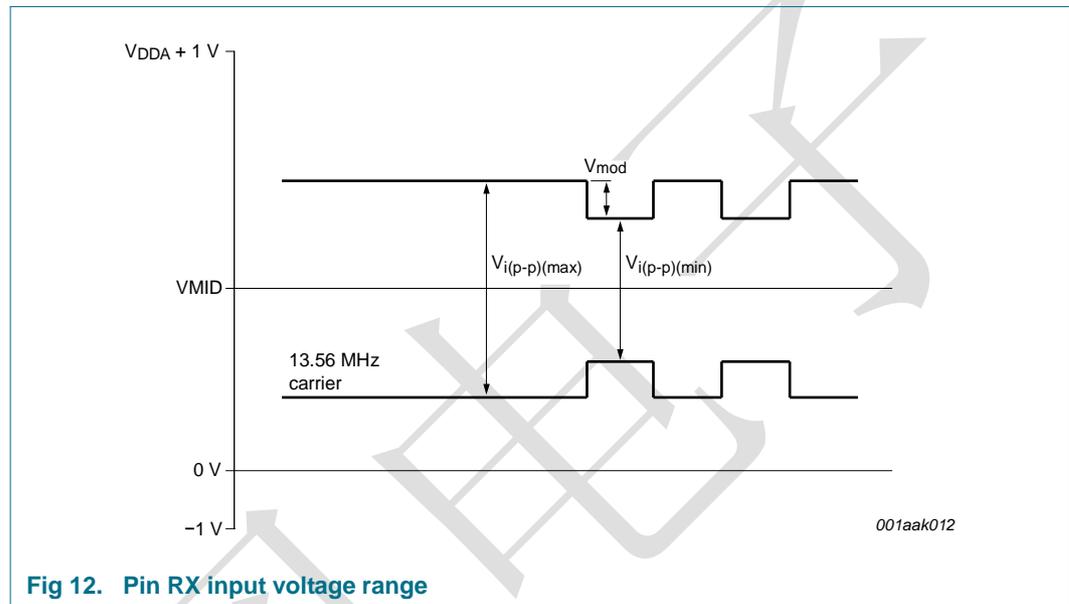
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>OH</sub>	HIGH-level output voltage	V <sub>DD(PVDD)</sub> = 3 V; I <sub>O</sub> = 4 mA	V <sub>DD(PVDD)</sub> - 0.4	-	V <sub>DD(PVDD)</sub>	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>DD(PVDD)</sub> = 3 V; I <sub>O</sub> = 4 mA	V <sub>SS(PVSS)</sub>	-	V <sub>SS(PVSS)</sub> + 0.4	V
I <sub>OH</sub>	HIGH-level output current	V <sub>DD(PVDD)</sub> = 3 V	-	-	4	mA
I <sub>OL</sub>	LOW-level output current	V <sub>DD(PVDD)</sub> = 3 V	-	-	4	mA
<b>Output characteristics</b>						
<b>Pin MFOUT</b>						
V <sub>OH</sub>	HIGH-level output voltage	V <sub>DD(SVDD)</sub> = 3 V; I <sub>O</sub> = 4 mA	V <sub>DD(SVDD)</sub> - 0.4	-	V <sub>DD(SVDD)</sub>	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>DD(SVDD)</sub> = 3 V; I <sub>O</sub> = 4 mA	V <sub>SS(PVSS)</sub>	-	V <sub>SS(PVSS)</sub> + 0.4	V
I <sub>OL</sub>	LOW-level output current	V <sub>DD(SVDD)</sub> = 3 V	-	-	4	mA
I <sub>OH</sub>	HIGH-level output current	V <sub>DD(SVDD)</sub> = 3 V	-	-	4	mA
<b>Pin IRQ</b>						
V <sub>OH</sub>	HIGH-level output voltage	V <sub>DD(PVDD)</sub> = 3 V; I <sub>O</sub> = 4 mA	V <sub>DD(PVDD)</sub> - 0.4	-	V <sub>DD(PVDD)</sub>	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>DD(PVDD)</sub> = 3 V; I <sub>O</sub> = 4 mA	V <sub>SS(PVSS)</sub>	-	V <sub>SS(PVSS)</sub> + 0.4	V
I <sub>OL</sub>	LOW-level output current	V <sub>DD(PVDD)</sub> = 3 V	-	-	4	mA
I <sub>OH</sub>	HIGH-level output current	V <sub>DD(PVDD)</sub> = 3 V	-	-	4	mA
<b>Pins AUX1 and AUX2</b>						
V <sub>OH</sub>	HIGH-level output voltage	V <sub>DDD</sub> = 3 V; I <sub>O</sub> = 4 mA	V <sub>DDD</sub> - 0.4	-	V <sub>DDD</sub>	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>DDD</sub> = 3 V; I <sub>O</sub> = 4 mA	V <sub>SS(PVSS)</sub>	-	V <sub>SS(PVSS)</sub> + 0.4	V
I <sub>OL</sub>	LOW-level output current	V <sub>DDD</sub> = 3 V	-	-	4	mA
I <sub>OH</sub>	HIGH-level output current	V <sub>DDD</sub> = 3 V	-	-	4	mA
<b>Pins TX1 and TX2</b>						
V <sub>OH</sub>	HIGH-level output voltage	V <sub>DD(TVDD)</sub> = 3 V; I <sub>DD(TVDD)</sub> = 32 mA; CWGsP[5:0] = 3Fh	V <sub>DD(TVDD)</sub> - 0.15	-	-	V
		V <sub>DD(TVDD)</sub> = 3 V; I <sub>DD(TVDD)</sub> = 80 mA; CWGsP[5:0] = 3Fh	V <sub>DD(TVDD)</sub> - 0.4	-	-	V
		V <sub>DD(TVDD)</sub> = 2.5 V; I <sub>DD(TVDD)</sub> = 32 mA; CWGsP[5:0] = 3Fh	V <sub>DD(TVDD)</sub> - 0.24	-	-	V
		V <sub>DD(TVDD)</sub> = 2.5 V; I <sub>DD(TVDD)</sub> = 80 mA; CWGsP[5:0] = 3Fh	V <sub>DD(TVDD)</sub> - 0.64	-	-	V

Table 144. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V <sub>OL</sub>	LOW-level output voltage	V <sub>DD(TVDD)</sub> = 3 V; I <sub>DD(TVDD)</sub> = 32 mA; CWGsP[5:0] = 0Fh	-	-	0.15	V	
		V <sub>DD(TVDD)</sub> = 3 V; I <sub>DD(TVDD)</sub> = 80 mA; CWGsP[5:0] = 0Fh	-	-	0.4	V	
		V <sub>DD(TVDD)</sub> = 2.5 V; I <sub>DD(TVDD)</sub> = 32 mA; CWGsP[5:0] = 0Fh	-	-	0.24	V	
		V <sub>DD(TVDD)</sub> = 2.5 V; I <sub>DD(TVDD)</sub> = 80 mA; CWGsP[5:0] = 0Fh	-	-	0.64	V	
<b>Current consumption</b>							
I <sub>pd</sub>	power-down current	V <sub>D<sub>DA</sub></sub> = V <sub>D<sub>DD</sub></sub> = V <sub>DD(TVDD)</sub> = V <sub>DD(PVDD)</sub> = 3 V					
		hard power-down; pin NRSTPD set LOW	[2]	-	-	5	μA
		soft power-down; RF level detector on	[2]	-	-	10	μA
I <sub>DD</sub>	digital supply current	pin DVDD; V <sub>D<sub>DD</sub></sub> = 3 V	-	6.5	9	mA	
I <sub>D<sub>DA</sub></sub>	analog supply current	pin AVDD; V <sub>D<sub>DA</sub></sub> = 3 V; CommandReg register's bit RcvOff = 0	-	7	10	mA	
		pin AVDD; receiver switched off; V <sub>D<sub>DA</sub></sub> = 3 V; CommandReg register's bit RcvOff = 1	-	3	5	mA	
I <sub>DD(PVDD)</sub>	PVDD supply current	pin PVDD	[3]	-	40	mA	
I <sub>DD(TVDD)</sub>	TVDD supply current	pin TVDD; continuous wave	[4][5][6]	-	60	100	mA
I <sub>DD(SVDD)</sub>	SVDD supply current	pin SVDD	[7]	-	4	mA	
<b>Clock frequency</b>							
f <sub>clk</sub>	clock frequency		-	27.12	-	MHz	
δ <sub>clk</sub>	clock duty cycle		40	50	60	%	
t <sub>jit</sub>	jitter time	RMS	-	-	10	ps	
<b>Crystal oscillator</b>							
V <sub>OH</sub>	HIGH-level output voltage	pin OSCOUT	-	1.1	-	V	
V <sub>OL</sub>	LOW-level output voltage	pin OSCOUT	-	0.2	-	V	
C <sub>i</sub>	input capacitance	pin OSCOUT	-	2	-	pF	
		pin OSCIN	-	2	-	pF	
<b>Typical input requirements</b>							
f <sub>xtal</sub>	crystal frequency		-	27.12	-	MHz	
ESR	equivalent series resistance		-	-	100	Ω	
C <sub>L</sub>	load capacitance		-	10	-	pF	
P <sub>xtal</sub>	crystal power dissipation		-	50	100	mW	

[1] The voltage on pin RX is clamped by internal diodes to pins AVSS and AVDD.

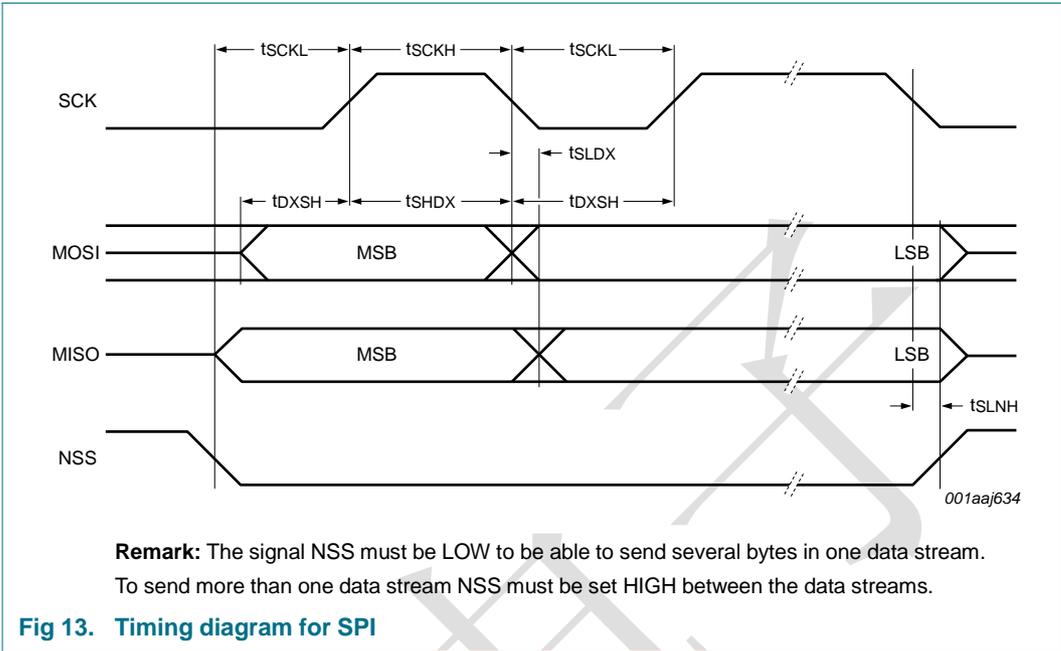
- [2]  $I_{pd}$  is the total current for all supplies.
- [3]  $I_{DD(PVDD)}$  depends on the overall load at the digital pins.
- [4]  $I_{DD(TVDD)}$  depends on  $V_{DD(TVDD)}$  and the external circuit connected to pins TX1 and TX2.
- [5] During typical circuit operation, the overall current is below 100 mA.
- [6] Typical value using a complementary driver configuration and an antenna matched to  $40\ \Omega$  between pins TX1 and TX2 at 13.56 MHz.
- [7]  $I_{DD(SVDD)}$  depends on the load at pin MFOUT.



## 14.1 Timing characteristics

**Table 145. SPI timing characteristics**

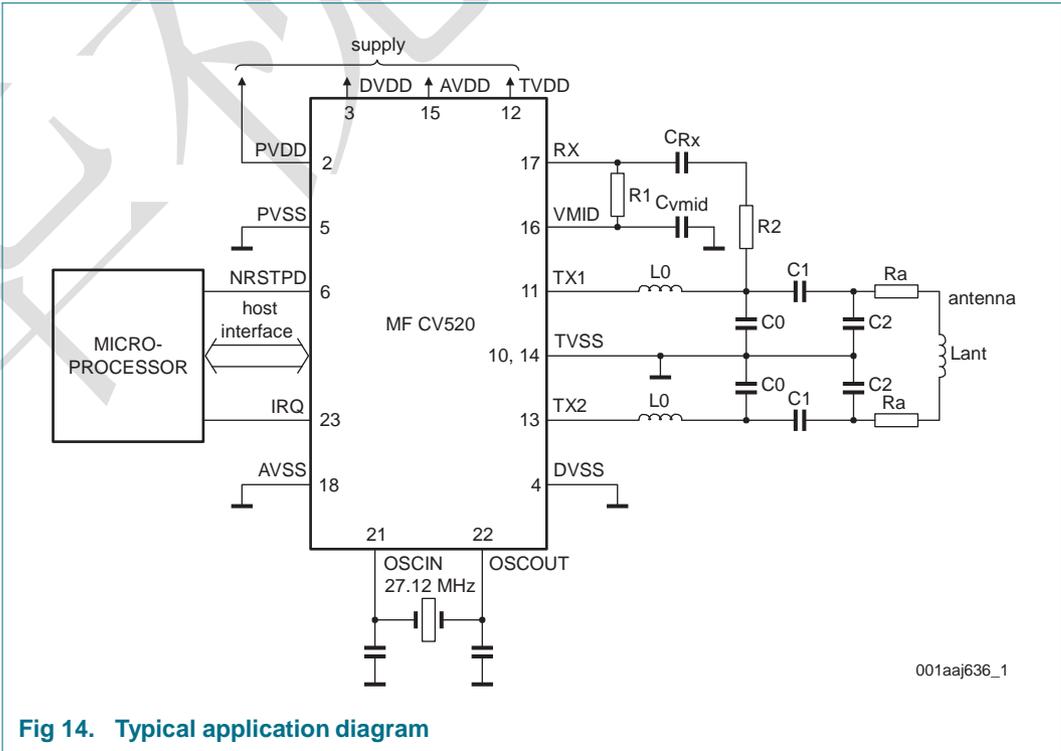
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{WL}$	pulse width LOW	line SCK	50	-	-	ns
$t_{WH}$	pulse width HIGH	line SCK	50	-	-	ns
$t_{h(SCKH-D)}$	SCK HIGH to data input hold time	SCK to changing MOSI	25	-	-	ns
$t_{su(D-SCKH)}$	data input to SCK HIGH set-up time	changing MOSI to SCK	25	-	-	ns
$t_{h(SCKL-Q)}$	SCK LOW to data output hold time	SCK to changing MISO	-	-	25	ns
$t_{(SCKL-NSSH)}$	SCK LOW to NSS HIGH time		0	-	-	ns
$t_{NHNL}$	NSS high before communication		50	-	-	ns



### 15. Application information

A typical application diagram using a complementary antenna connection to the MF CV520 is shown in [Figure 14](#).

The antenna tuning and RF part matching is described in the application note [Ref. 1](#) and [Ref. 2](#).



## 16. Test information

### 16.1 Test signals

#### 16.1.1 Self test

The MF CV520 has the capability to perform a digital self test. The self test is started by using the following procedure:

1. Perform a soft reset.
2. Clear the internal buffer by writing 25 bytes of 00h and implement the Config command.
3. Enable the self test by writing 09h to the AutoTestReg register.
4. Write 00h to the FIFO buffer.
5. Start the self test with the CalcCRC command.
6. The self test is initiated.
7. When the self test has completed, the FIFO buffer contains the following 64 bytes:

FIFO buffer byte values for version 92h:

0x00, 0xEB, 0x66, 0xBA, 0x57, 0xBF, 0x23, 0x95, 0xD0, 0xE3, 0x0D, 0x3D, 0x27, 0x89, 0x5C, 0xDE, 0x9D, 0x3B, 0xA7, 0x00, 0x21, 0x5B, 0x89, 0x82, 0x51, 0x3A, 0xEB, 0x02, 0x0C, 0xA5, 0x00, 0x49, 0x7C, 0x84, 0x4D, 0xB3, 0xCC, 0xD2, 0x1B, 0x81, 0x5D, 0x48, 0x76, 0xD5, 0x71, 0x61, 0x21, 0xA9, 0x86, 0x96, 0x83, 0x38, 0xCF, 0x9D, 0x5B, 0x6D, 0xDC, 0x15, 0xBA, 0x3E, 0x7D, 0x95, 0x3B, 0x2F

#### 16.1.2 Test bus

The test bus is used for production tests. The following configuration can be used to improve the design of a system using the MF CV520. The test bus allows internal signals to be routed to the digital interface. The test bus comprises two sets of test signals which are selected using their subaddress specified in the TestSel2Reg register's TestBusSel[4:0] bits. The test signals and their related digital output pins are described in [Table 146](#) and [Table 147](#).

**Table 146. Test bus signals: TestBusSel[4:0] = 07h**

Pins	Internal signal name	Description
D6	s_data	received data stream
D5	s_coll	bit-collision detected (106 kBd only)
D4	s_valid	s_data and s_coll signals are valid
D3	s_over	receiver has detected a stop condition
D2	RCV_reset	receiver is reset
D1	-	reserved

**Table 147. Test bus signals: TestBusSel[4:0] = 0Dh**

Pins	Internal test signal name	Description
D6	clkstable	oscillator output signal
D5	clk27/8	oscillator output signal divided by 8
D4 to D3	-	reserved
D2	clk27	oscillator output signal
D1	-	reserved

### 16.1.3 Test signals on pins AUX1 or AUX2

The MF CV520 allows the user to select internal signals for measurement on pins AUX1 or AUX2. These measurements can be helpful during the design-in phase to optimize the design or used for test purposes.

[Table 148](#) shows the signals that can be switched to pin AUX1 or AUX2 by setting AnalogSelAux1[3:0] or AnalogSelAux2[3:0] in the AnalogTestReg register.

**Remark:** The DAC has a current output, therefore it is recommended that a 1 k $\Omega$  pull-down resistor is connected to pin AUX1 or AUX2.

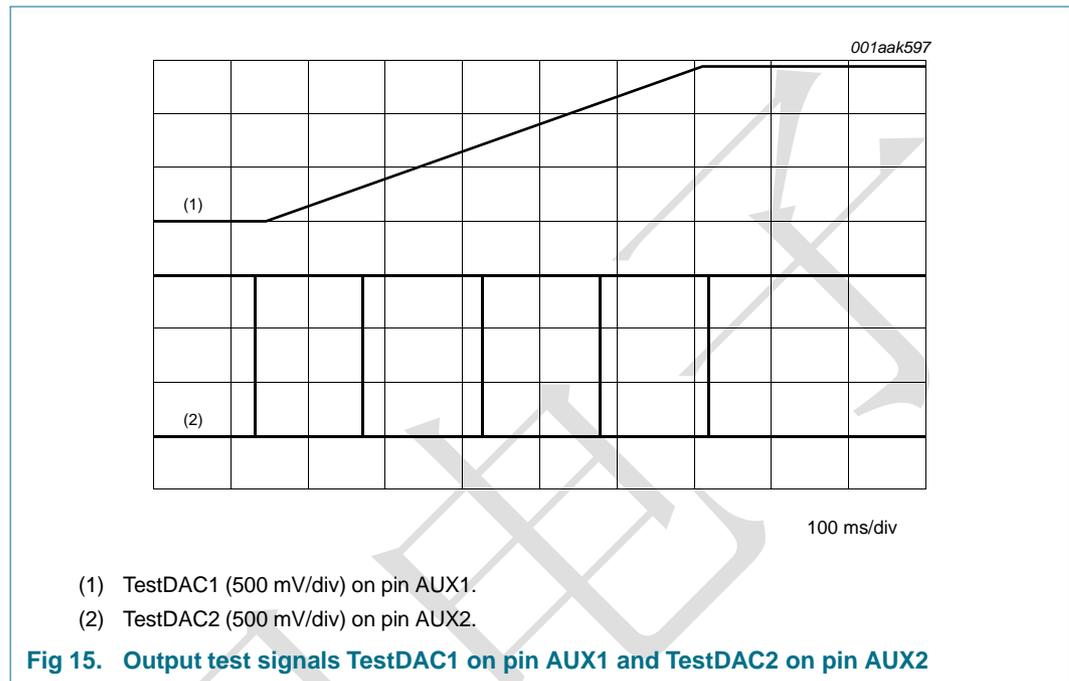
**Table 148. Test signal descriptions**

AnalogSelAux1[3:0] or AnalogSelAux2[3:0] value	Signal on pin AUX1 or pin AUX2
0000	3-state
0001	DAC: register TestDAC1 or TestDAC2
0010	DAC: test signal Corr1
0011	reserved
0100	DAC: test signal MinLevel
0101	DAC: test signal ADC_I
0110	DAC: test signal ADC_Q
0111 to 1001	reserved
1010	HIGH
1011	LOW
1100	TxActive
1101	RxActive
1110	subcarrier detected
1111	TstBusBit

#### 16.1.3.1 Example: Output test signals TestDAC1 and TestDAC2

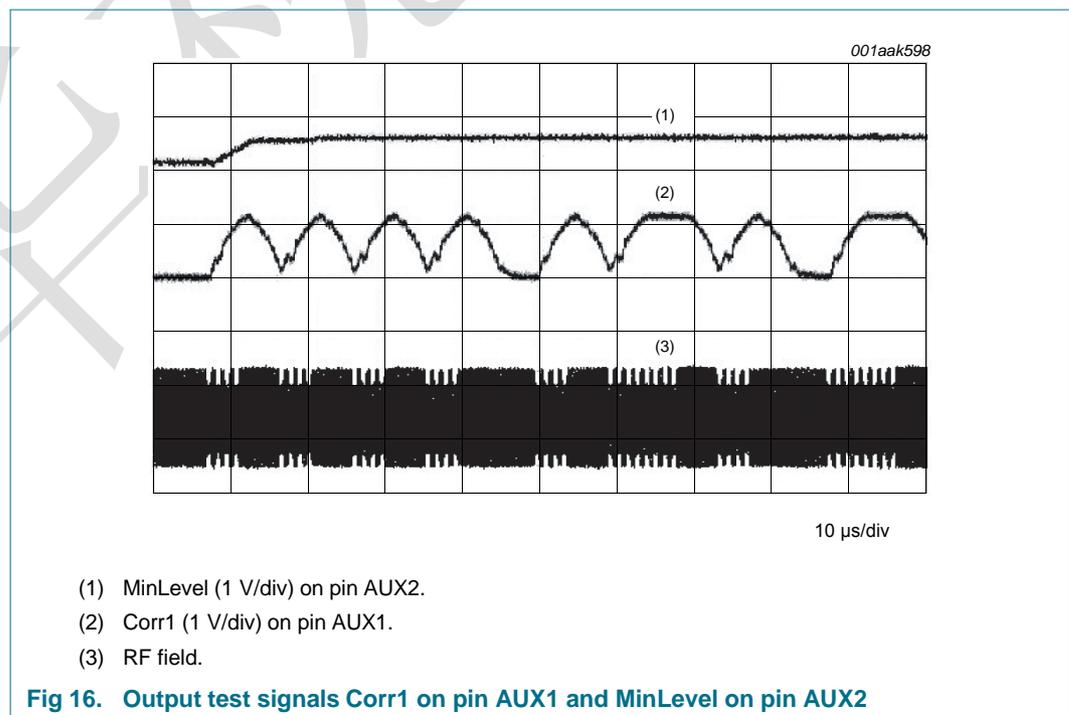
The AnalogTestReg register is set to 11h. The output on pin AUX1 has the test signal TestDAC1 and the output on pin AUX2 has the test signal TestDAC2. The signal values of TestDAC1 and TestDAC2 are controlled by the TestDAC1Reg and TestDAC2Reg registers.

Figure 15 shows test signal TestDAC1 on pin AUX1 and TestDAC2 on pin AUX2 when the TestDAC1Reg register is programmed with a slope defined by values 00h to 3Fh and the TestDAC2Reg register is programmed with a rectangular signal defined by values 00h and 3Fh.



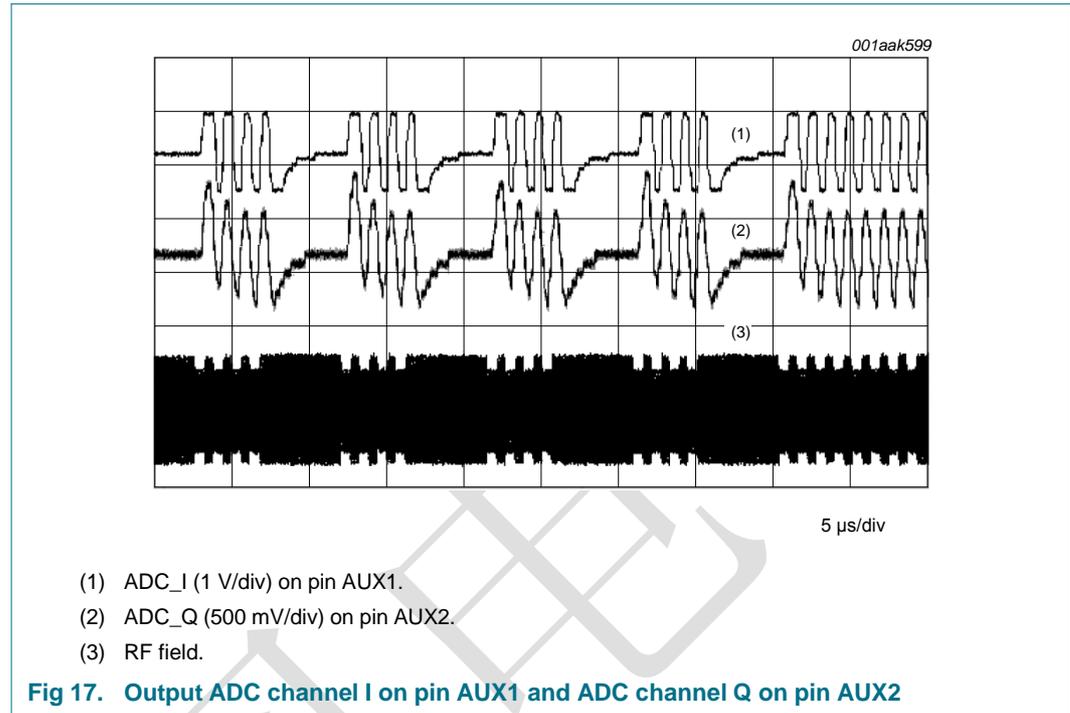
### 16.1.3.2 Example: Output test signals Corr1 and MinLevel

Figure 16 shows test signals Corr1 and MinLevel on pins AUX1 and AUX2, respectively. The AnalogTestReg register is set to 24h.



### 16.1.3.3 Example: Output test signals ADC channel I and ADC channel Q

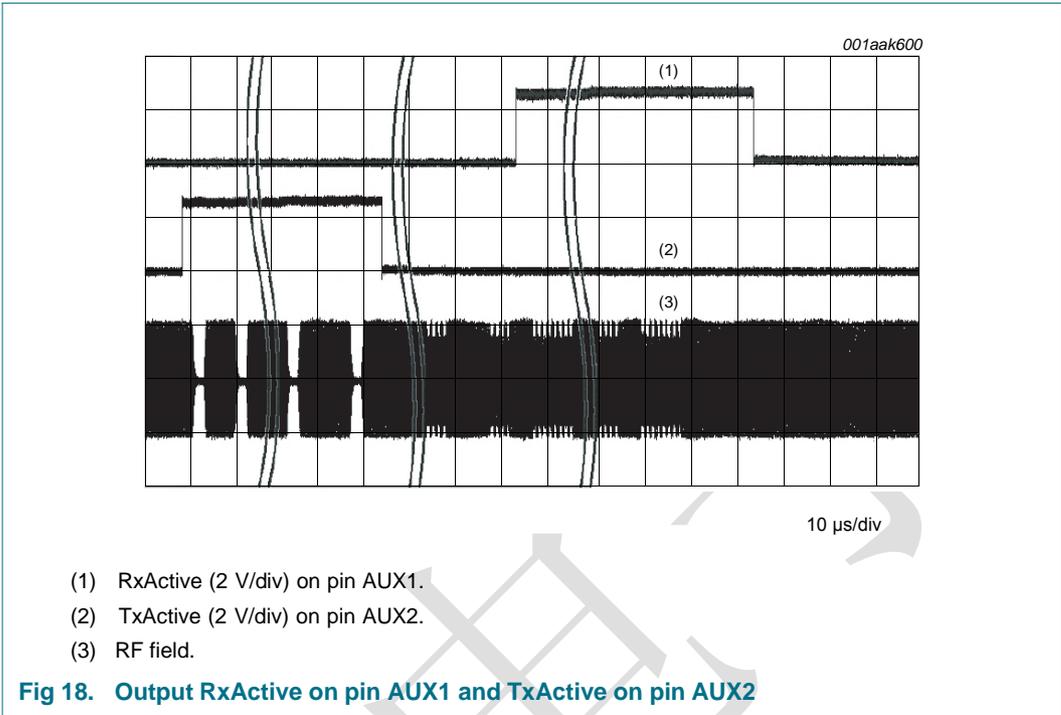
[Figure 17](#) shows the channel behavior test signals ADC\_I and ADC\_Q on pins AUX1 and AUX2, respectively. The AnalogTestReg register is set to 56h.



### 16.1.3.4 Example: Output test signals RxActive and TxActive

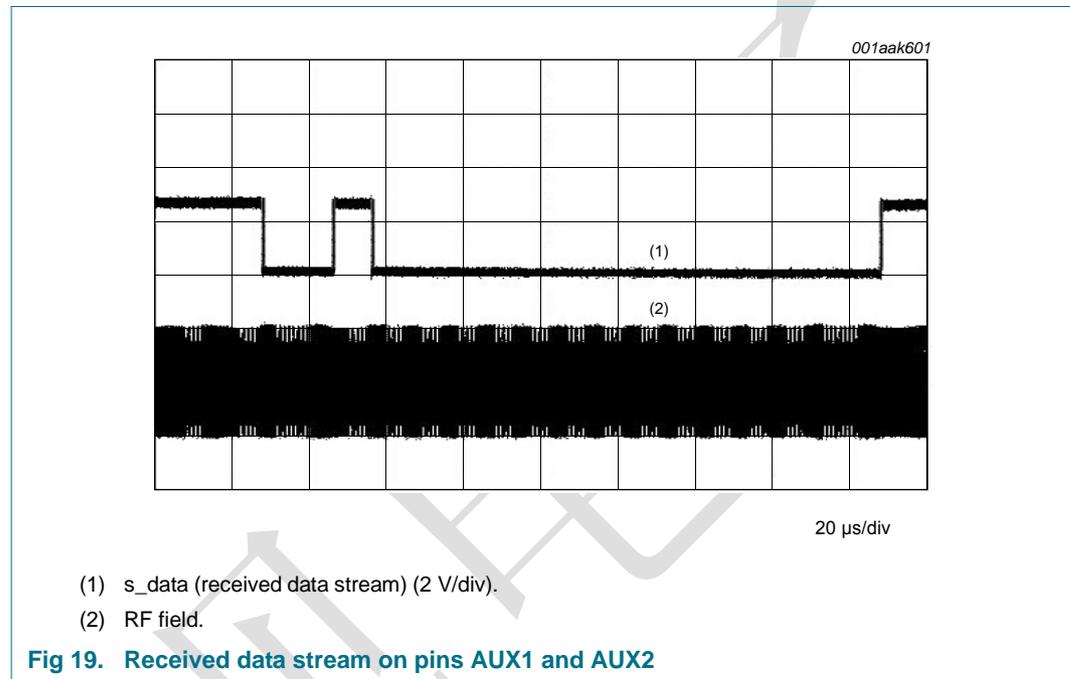
[Figure 18](#) shows the RxActive and TxActive test signals relating to RF communication. The AnalogTestReg register is set to CDh.

- At 106 kBd, RxActive is HIGH during data bits, parity and CRC reception. Start bits are not included
- At 106 kBd, TxActive is HIGH during start bits, data bits, parity and CRC transmission
- At 212 kBd, 424 kBd and 848 kBd, RxActive is HIGH during data bits and CRC reception. Start bits are not included
- At 212 kBd, 424 kBd and 848 kBd, TxActive is HIGH during data bits and CRC transmission



### 16.1.3.5 Example: Output test signal RX data stream

Figure 19 shows the data stream that is currently being received. The TestSel2Reg register's TestBusSel[4:0] bits are set to 07h to enable test bus signals on pins D1 to D6; see Section 16.1.2 on page 63. The TestSel1Reg register's TstBusBitSel[2:0] bits are set to 06h (pin D6 = s\_data) and AnalogTestReg register is set to FFh (TstBusBit) which outputs the received data stream on pins AUX1 and AUX2.



### 16.1.3.6 PRBS

The pseudo-random binary sequences PRBS9 and PRBS15 are based on ITU-T0150 and are defined with the TestSel2Reg register. Transmission of either data stream is started by the Transmit command. The preamble/sync byte/start bit/parity bit are automatically generated depending on the mode selected.

**Remark:** All relevant registers for transmitting data must be configured in accordance with ITU-T0150 before selecting PRBS transmission.

# 17. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm

SOT617-1

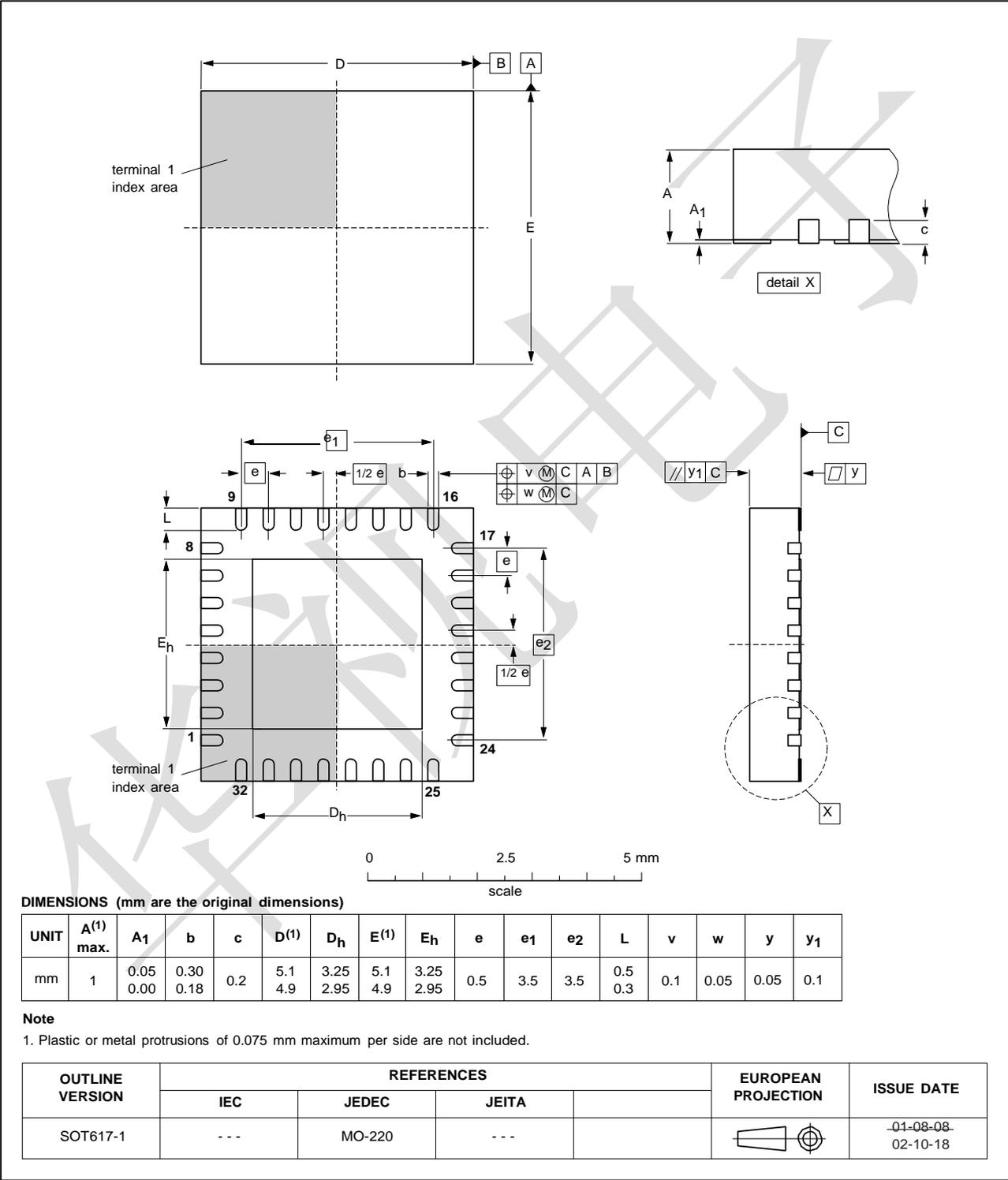


Fig 20. Package outline SOT617-1 (HVQFN32)

Detailed package information can be found at:  
<http://www.nxp.com/package/SOT617-1.html>.

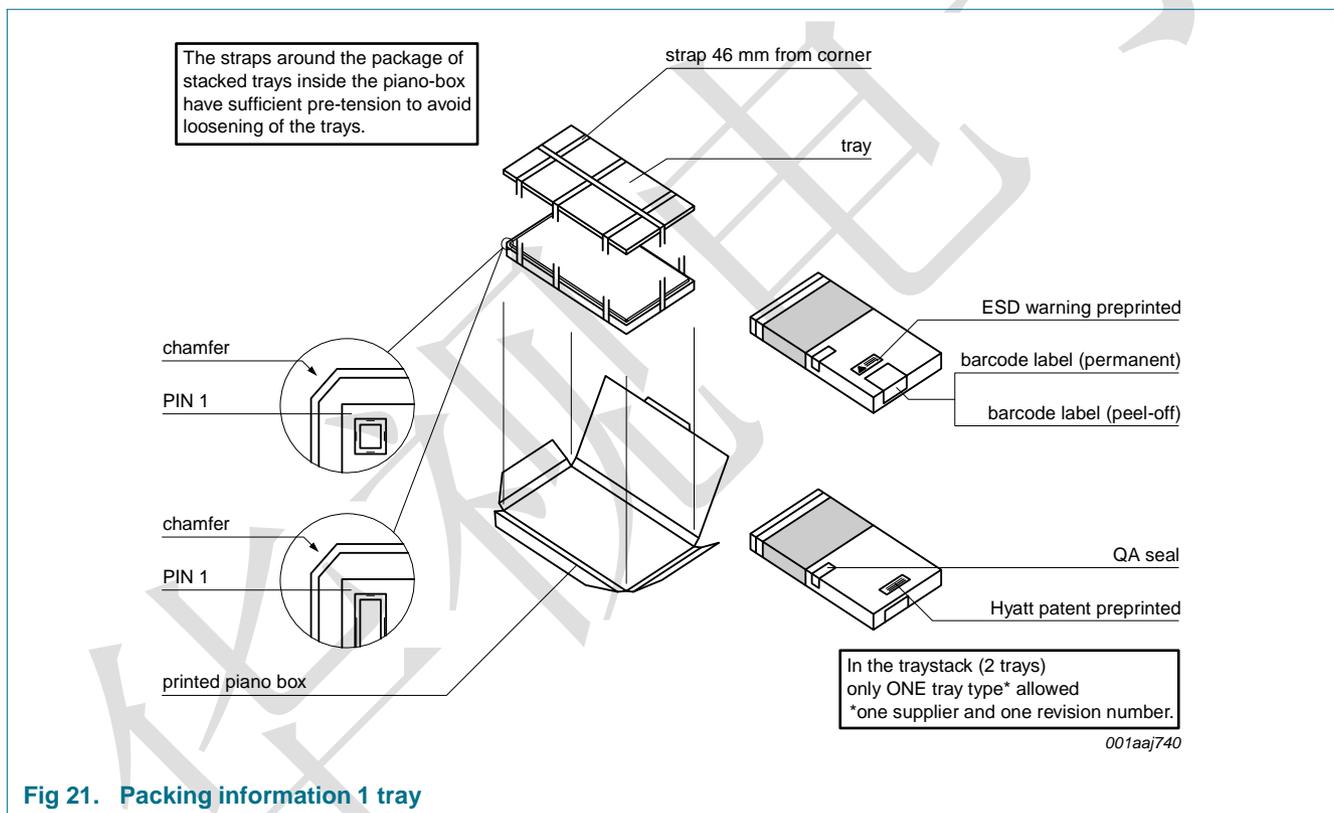
## 18. Handling information

Moisture Sensitivity Level (MSL) evaluation has been performed according to *SNW-FQ-225B rev.04/07/07 (JEDEC J-STD-020C)*. MSL for this package is level 1 which means 260 °C convection reflow temperature.

Dry pack is not required.

Unlimited out-of-pack floor life at maximum ambient 30 °C/85 % RH.

## 19. Packing information



## 20. Abbreviations

**Table 149. Abbreviations**

Acronym	Description
ADC	Analog-to-Digital Converter
BPSK	Binary Phase Shift Keying
CRC	Cyclic Redundancy Check
CW	Continuous Wave
DAC	Digital-to-Analog Converter
HBM	Human Body Model
LSB	Least Significant Bit
MISO	Master In Slave Out
MM	Machine Model
MOSI	Master Out Slave In
MSB	Most Significant Bit
NRZ	Not Return to Zero
NSS	Not Slave Select
PLL	Phase-Locked Loop
PRBS	Pseudo-Random Bit Sequence
RX	Receiver
SOF	Start Of Frame
SPI	Serial Peripheral Interface
TX	Transmitter
UART	Universal Asynchronous Receiver Transmitter

## 21. References

- [1] **Application note** — *MFRC52x Reader IC Family Directly Matched Antenna Design*
- [2] **Application note** — *MIFARE (ISO/IEC 14443 A) 13.56 MHz RFID Proximity Antennas*

## 22. Revision history

Table 150. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
MF CV520_219710	20111213	Product data sheet	-	-

## 23. Legal information

### 23.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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